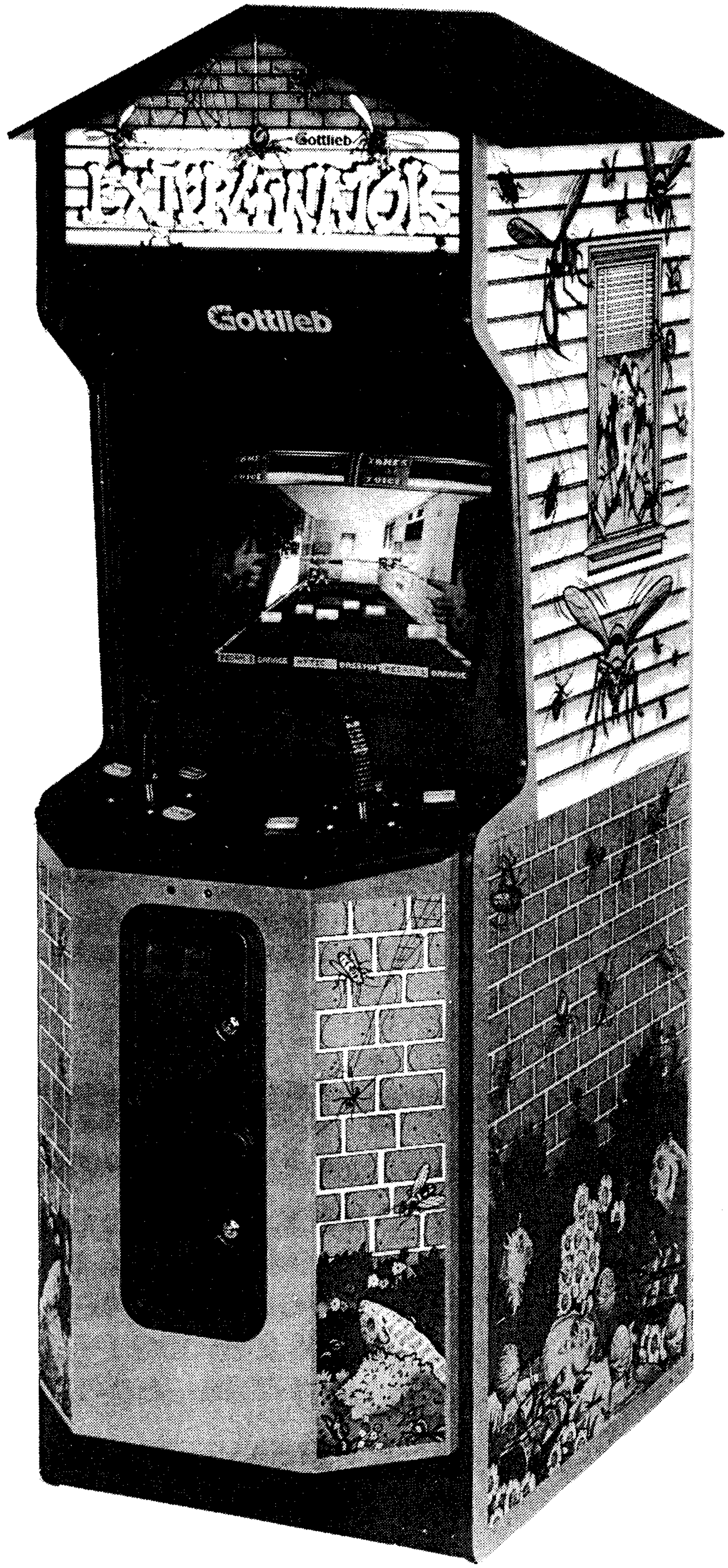
Gottlieb®



INSTRUCTION MANUAL

EXTERMINATOR (GAME #V101)
INSTRUCTION MANUAL

TABLE OF CONTENTS

Premier®
Technology

759 INDUSTRIAL DRIVE
BENSENVILLE, IL 60106
1-708-350-0400
TELEX 215009 PRMR
FAX: 1-708-350-1097

THE PREMIER HOTLINE
1-800-444-0761

"**WARNING:** This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instructions manual, may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference."

Premier ®
Technology

VIDEO SYSTEM OVERVIEW

The Exterminator video system is a state of the art video graphic system utilizing the latest in video graphics technology to provide color resolution never before seen in a video game!

The heart of the system is two Texas Instruments 34010 Graphics System Processor chips (GSPs) running at 40Mhz. these general purpose micro-processors control the game flow and the video timing.

There are 2 bitmapped video planes, a foreground and a background. The foreground plane has a pixel resolution of 256 X 240 pixels at 8 bits per pixel (or 256 colors). The background plane has the same pixel resolution as the foreground, but with a color resolution of 16 bits per pixel (or 32,768 colors). The foreground plane is strictly color-mapped, while in the background, each pixel has the option of containing its own color map of up to 2048 colors.

Images and program are stored in ROMS with a total potential capacity of 2MB of storage.

One GSP is used as a Master. This GSP controls the game logic as well as the background plane. All ROM is available to the Master GSP, along with 512 KB of scratch RAM. The other GSP functions as a Slave, controlling only the foreground screen. This GSP has 1 MB of RAM available to it. All program and image data is downloaded to the Slave GSP from the Master before the Slave can function.

Backup memory is provided by a EEPROM chip which retains all bookkeeping information along with coin counts and game adjustments when power is shut off. No batteries are needed.

A JAMMA connector supplies all the standard JAMMA signals, while separate ports allow for additional signals to be supplied to the processor. In all, 30 player input lines are available.

A diagnostic connector is supplied to enable a host computer to download diagnostic programs and perform tests on the video board in the field. (This feature will be made available some time in the future).

I. INSTALLATION

A. SET-UP

1. Carefully inspect the exterior of the game for any damage which might have occurred during shipment.

2. Unlock and open the rear cabinet door.

3. Check that all plug-in connectors are seated firmly. The connectors are keyed so they will only go in one way.

4. Remove the binding strap from the line cord, and install the line cord plate in the groove provided.

5. Adjust the (4) attached cabinet levelers as required.

B. CHECK-UP

1. Check that all cables are free of moving parts.

2. Check for any loose wires.

3. Check for loose solder or foreign matter on switches and power supply assemblies.

4. Be certain all fuses are seated firmly.

5. Be sure transformer wiring corresponds to the supply voltage.

6. Refer to section VI to make all the necessary game adjustments.

7. Reassemble the game.

8. Plug the line cord into a properly grounded 3-wire receptacle ONLY!!

C. CONTROL PANEL REMOVAL

1. Unplug the game.

2. Unlock and open the coin chute door.

3. Reach in through the coin chute door and unsnap the (2) latches located on the left and right sides. Grasp the two joysticks and with a concurrent motion of pushing the control panel forward 1/8" and lifting up at the rear of the panel while it pivots on the front edge of the control panel to clear the lockdown bracket. Disconnect cable connectors A9P1/A9J1 and A9P2/A9J2.

4. Remove the entire control panel assembly from the game.

5. The joystick and micro switches now accessible for removal or cleaning.

D. MONITOR REMOVAL

1. Unplug the game.

2. Perform the control panel assembly removal procedure (Section C).

3. Unlock and open the rear cabinet door.

4. Lift up the video glass 1/4" to clear the retaining slot and set aside.

5. Remove the (6) Phillips head screws and carefully remove and set aside the monitor mask.

6. NOTE: the color monitor contains HIGH VOLTAGES delivering LETHAL quantities of energy. Do not attempt to service the monitor until you have shorted the anode plug on the picture tube to ground.

7. Disconnect the two cable connectors A10P4/A10J4 and A12P9/A12J9 mounted on the rear walls of the cabinet.

8. Disconnect A3J1 from the monitor PC board and cable connector A12P3/A12J3. Remove the ground straps mounted on the monitor frame. Remove the monitor front control board mounted on the lower right side.

9. Remove the (4) Hex nuts and washers attached to the carriage bolts mounted on each side of the cabinet. Carefully grasp the monitor assembly which includes the wood front mounting and slide it down the wood rails being careful to clear the cables mounted on each side of the cabinet walls

E. MARQUEE ACCESS

1. Remove the (3) button head allen screws to detach the marquee support bracket, remove the screened marquee and set aside.

II. INITIALIZATION

POWER ON...

The power on process normally takes about 5 seconds. During this time, the screen will show an indeterminate pattern. After a successful initialization, the demo portion of the attract mode will begin.

If there is a problem with the backup memory (EEPROM), then one of 3 things may occur...

1) If the EEPROM socket is empty (that is, no EEPROM chip is present) a message will be displayed saying "WARNING! NO EEPROM CHIP IS PRESENT. BOOKKEEPING TOTALS AND GAME ADJUSTMENTS WILL BE LOST WHEN GAME IS POWERED DOWN." The game will function normally, but any information normally stored in EEPROM is initialized to default values. (See section on EEPROM)

2) If some adjustment parameter is found to be invalid, the message "WARNING! ADJUSTMENTS NEED TO BE RESET. TURN GAME OFF, THEN ON, THEN INFORM SERVICEMAN." will appear. Turning the game off and on should allow the game to start normally, however, you should check the game adjustments to make sure they are set the way you want.

3) If the EEPROM is found to have invalid data, or if a new EEPROM has just been installed, the message "INITIALIZING EEPROM....PLEASE WAIT" will appear. The initialization will take about 12 seconds and then the demo part of the attract mode will begin.

III. GAME OPERATION

A. GAME START

1. Insert coins into coin chute.
   a. Coin chute sound is played.
   b. Total credits are displayed on the screen.

2. Press either start button to start a game.
   a. Total credits are decreased by one or two depending on the game adjustment setting.
   b. A demonstration scene is displayed on the screen. This demonstration can be cut short by pressing the start button again.
   c. The game begins.

B. SECOND PLAYER

1. A second player may enter the game at any time by pressing the manual start button.

C. GAME CONTINUATION

1. A player has ten seconds to continue his game after his bug juice has run dry. Pressing the start button within this time will allow him to proceed with play from his current house and room.

IV. SOUND/SPEECH

ATTRACT MODE

SOUND	OCCURRENCE
Theme music	When the Exterminator logo is built on the screen.
Typewriter	When the bug crawls back and forth leaving game instructions.
Assorted sounds	During the sample play scene in the kitchen.

SPEECH	OCCURRENCE
"Help me"	Speaks every other time the word "Help" appears by a house.

NOTE: The above attract mode sounds can be turned off by setting the attract sound game adjustment to "No".

GAME MODE

SPEECH	OCCURRENCE
"Ouch"	Whenever the hand gets stung, bitten or shot.

V. GAME PLAY AND SCORING

HOW TO PLAY... EXTERMINATOR™

In this game, you are a Pest Control Expert sent to a neighborhood to rid it of assorted pests. You are a disembodied hand with a number of skills at your disposal...you can squish enemies by getting them in your palm and closing your hand, you can pound enemies on the ground, and you can shoot enemies by squirting a toxic pesticide out of your finger.

The neighborhood consists of 7 houses, each house having 5 rooms. The combination of rooms is different in each house, and the combinations of enemies are different in each house.

Enemies which cannot harm you are the flies, ants, spiders, gubbers (green bats), nuts, cans, and tomatoes. Enemies which CAN harm you are the wasp, dragonflies, toads, mosquitoes, tanks and squirt bottle. Some enemies appear only on the ground. Others appear only in the air. You can only pound ground enemies, and you can either shoot or squish flying enemies. Table 1 shows the wave structure of the game.

When the game begins, your "JUICE" gauge reads full. Any number of things can rob you of juice. Some things can restore your juice. The game ends when you run out of juice. If you want to continue playing, you can drop in another coin and receive full JUICE again. The only time you cannot immediately continue playing when you run out of juice is during the Ultimate Challenge, which is explained later.

Dangerous enemies each have different characteristics and need to be handled differently. All flying enemies can be shot. All ground enemies can be pounded.

WASP - The wasp will seek out your hand and then sting you. If you squish it, you will get stung anyway. Being stung will rob you of some juice. If a wasp is hovering around you, shake your hand (by shaking the joystick) to make it go away. Shooting it will delay another wasp from seeking you.

MOSQUITOES - The mosquitoes seek you out and bite you. This also robs you of your juice. Shaking has no effect on them, but you can squish them without harm.

DRAGONFLIES - Dragonflies can be squished without harm also, but they randomly drop bombs which zap you (and take away some juice) when they explode. If you grab a bomb BEFORE it explodes you RECEIVE a small amount of juice.

TOY TANKS - The tanks fire live ammo. If your hand is hit, you lose some juice. Tanks can be pounded.

TOADS - The toads will shoot their tongues out and suck you into their mouths. This will also cause a loss of juice. Toads can also be pounded.

SQUIRT BOTTLE - The squirt bottle shoots juice back at you. If you get hit, you lose some juice.
It never shoots while it is

moving, and it only moves when you move towards it. If you CAN grab it, you receive some juice.

In addition to all the enemies, there is a glowing dodecahedron which (if grabbed) will supply you with some extra juice. This dodecahedron is not harmful to you in any way.

You always have the choice of which skill to use at any given time. To shoot, make sure your hand is all the way over to your side of the screen (Left for the left player, Right for the right player). When this is done, the hand moves into a shooting position (forefinger pointing only). Now when the joystick button is pressed, the hand will fire. Rotating the stick and moving it up and down will allow aiming to every part of the room except directly across to where the other player is.

Moving the hand toward the center of the screen while the button is released causes the hand to open. Now when the joystick button is pressed, the hand will close, squishing anything in its grasp.

The pound button will cause the hand to pound onto the ground. The hand must be at a certain minimum height for pounding to work. If the hand is too low, a message flashes on saying "TOO LOW TO POUND".

The floor of each room contains 6 lanes of tiles. When you squish, pound of shoot anything in the air (EXCEPT THE SQUIRT BOTTLE) it falls to the ground and changes the color of the tile it lands on. If the left (red) player shot it, the tile turns red. If the right (blue) player shot it, it turns blue. When an entire lane of tiles (from front to back) contains a single color, then that player has completed the room and won that wave. The next room is determined by which lane was completed. (Each lane is labelled with a room name depending on which rooms are left to be completed in that house).

When an enemy falls on a tile directly under your hand, the game will rotate that lane so the next tile which is NOT YOUR COLOR appears underneath your hand in that lane. This is done to make all your pounds and squishes work to your advantage.

BONUS ROUNDS

Some basement and kitchen waves are bonus rounds. Whichever player completes these rooms is entitled to 20 seconds of free gameplay to earn extra points. In the kitchen, the player can pound as many bugs and food items as possible within the 20 seconds. The basement gets turned into a shooting gallery with rats running up and down the shelves.

WARP FEATURE (optional feature)

In the kitchen waves of houses 1 and 3, the freezer door will open momentarily for an instant. If either player is shooting into the open freezer, gameplay will warp to the next house and the player (or players) who made the shot will be awarded 250,000 points.

ULTIMATE WAVE

After seven houses are completed, you find yourself outdoors and faced with an ultimate challenge. You must withstand the attacks of toads, dragonflies, mosquitoes and squirt bottles. In this wave, there are no tiles. Also, when an enemy is killed, it is not replenished (with exception of the squirt bottle, which can be very beneficial since grabbing it will give you juice and extend your life). To complete the wave, you must destroy all the enemies except the squirt bottle. First there is a wave of toads and dragonflies. When the

V. GAME PLAY AND SCORING

dragonflies are all gone, a wave of mosquitoes appears. If you run out of juice during this wave YOU CAN NOT CONTINUE PLAYING IN THIS WAVE! You must complete the last house again, before getting another chance at the ultimate wave.

ROUND PROGRESSION

House 1	Kitchen	Cans,Flies	
	Bedroom	Tanks,Gubbers	
	Attic	Ants,Gubbers	
	Garage	Ants,Mosquitoes	
	Basement	Tanks,Flies	(Bonus Round)
House 2	Garage	Frogs,Flies	
	Attic	Rats,Dragonflies	
	Basement	Rats,Spiders	(Bonus Round)
	Living Room	Ants,Mosquitoes	
House 3	Kitchen	Tomatoes,Dragonflies	(Bonus Round)
	Bedroom	Tanks,Mosquitoes	
	Living Room	Rats,Spiders	
	Attic	Frogs,Flies	
	Bathroom	Ants,Dragonflies	
House 4	Kitchen	Tomatoes,Dragonflies	(Bonus Round)
	Garage	Tanks,Mosquitoes	
	Basement	Frogs,Dragonflies	
	Bathroom	Frogs,Flies	
	Nursery	Rats,Mosquitoes	
House 5	Bedroom	Tanks,Gubbers	
	Attic	Tanks,Dragonflies	
	Living Room	Frogs,Mosquitoes	
	Bathroom	Ants,Mosquitoes	
	Nursery	Frogs,Dragonflies	
House 6	Kitchen	Frogs,Mosquitoes	(Bonus Round)
	Bedroom	Tanks,Mosquitoes	
	Basement	Frogs,Spiders	
	Living Room	Tanks,Dragonflies	
	Bathroom	Rats,Dragonflies	
House 7	Basement	Tanks,Dragonflies	(Bonus Round)
	Garage	Tanks,Mosquitoes	
	Attic	Rats,Flies	

Notes: The Wasp appears in every wave.
In House 1, the Spray Bottle appears in the Attic. But if completion of a room takes too long, it may appear in other rooms as well. In all other houses, the spray bottle will appear in all rooms.

V. GAME PLAY AND SCORING

SCORING

Shooting most Flying Enemies	750 Points
Shooting the Wasp	2000 Points
Squishing most Flying Enemies	1250 Points
Squishing the Squirt Bottle	5000 Points
Pounding most Ground Enemies	1250 Points
Warp to next house	250000 Points
Completion of Ultimate Wave	500000 Points
End of Wave bonus - Winning Player	1000 per Tile of your Color
End of Wave bonus - Losing Player	500 per Tile of you Color
Bonus Round - Basement	2500 per Rat
Bonus Round - Kitchen	1000 per Tomato 150 per Can 2000 per Nut 2500 per Ant

VI. GAME ADJUSTMENTS/OPTIONS

A. Video Board Assembly (A1) Switch Adjustments

Switch 1.............Not Used

Switches		Left Chute
2	3	Credits/Coin
Off	Off	1
On	Off	2
Off	On	3
On	On	4

Switches			Right Chute
4	5	6	Credits/Coin
Off	Off	Off	1
On	Off	Off	2
Off	On	Off	3
On	On	Off	4
Off	Off	On	5
On	Off	On	6
Off	On	On	7
On	On	On	8

Switch 7........Memory Tests
Off...............Single pass
On.........Continuous looping

Switch 8.........Normal/Free
Off...............Normal game
On..................Free play

B. SOUND ADJUSTMENTS

The audio output is controlled by the potentiometer mounted next to the service switch inside the coin mechanism door.

Turning the potentiometer counter-clockwise will decrease the volume. Turning it clockwise will increase the volume.

C. MONITOR ADJUSTMENTS

Normally, few if any adjustments are required for proper monitor operation. However, after any major repairs to the monitor chassis, refer to the attached monitor manual.

D. GAME ADJUSTMENTS

The following game adjustments are available:
Attract Sound - Yes or No
Credits/play - One or Two
Game difficulty - beginner, normal, hard, harder, and killer
Skill shot to advance house - Yes of No
These settings can be adjusted while in the bookkeeping and diagnostic mode.

VII. BOOKKEEPING AND SELF TEST

BOOKKEEPING
The bookkeeping functions of Exterminator are contained in Self Test step 1. These are in addition to the electromechanical coin counter located inside the cashbox access door. Every time a coin is inserted into either coin slot, the counter is energized to increment the count. The bookkeeping functions are triplicated for error correction and stored in an EEPROM on the video mother board at position U16.

SELF TEST
The self test consists of nine major functions which may be used to identify problems in the video and sound systems and to change program parameters.

The self test mode is entered by switching the toggle switch next to the volume control located inside the coin mech door. After a short wait, the menu of available tests is displayed on the monitor. To return to the game mode at any time, simply switch the toggle switch back to its original position while in any menu.

Selection of tests is done by using the left joystick to position the cursor next to the desired test and then momentarily pressing any left pound, start, or fire button. Once a test has been selected, the system will either begin the test or display a "submenu" showing additional test options.

Once a test is completed, the operator can return to the test menu by following the instructions on the monitor screen. The nine major test functions are as follows:

1. BOOKKEEPING
   Selecting the bookkeeping test displays a submenu allowing the operator a choice of five bookkeeping functions or the choice of returning to the main test menu. The subfunctions display the following information:

A. COIN COUNTERS. Seperate coin counters are maintained for the left and right coin chutes. Each coin counter maintains a long term value and a short term value. The short term values can be reset to zero by pressing the right start button together with either right pound button. The long term counts are not resetable and are maintained for the lifetime of the game. The left, right, and EOG adjusters along with EEPROM section pointer and EEPROM pass counter are internal functions and may provide helpful troubleshooting information for the Premier Technical Service Department.

B. WAVES & TIME RECORD. This display shows the highest, lowest, and average time played and waves completed per credit. By definition, a wave is a room in a house. This information can aid the operator in choosing the game difficulty setting. These records can be reset to zero by pressing both the right start and a right pound button together.

C. GAME ADJUSTMENTS. This screen shows the available game options and their present settings. The attract sound can be set "yes" or "no". Pricing choices are "1 credit/play" or "2 credits/play". Game difficulty options are "beginner", "normal", "hard", "harder", and "killer". Skill shot to advance house options are "yes" or "no". Game

adjustments can be changed by using the joystick to select a catagory and then pressing a left button to do the changing.

D. RESET HIGH SCORE TABLE. Resets all the high scores to their default values.

E. RESET ALL BUT HIGHEST SCORE. This choice leaves the highest score untouched and resets all others to their default values.

2. EPROM TEST
This test determines the condition of all EPROMs on the video mother board. The display shows the position of each EPROM on the board, its checksum calculated during the test, and if its calculated checksum is correct. Red indicates a bad EPROM, and green indicates good. A black EPROM position indicates an empty socket.

3. SCRATCH/STACK RAM TEST
Checks both the master and slave RAM. This test performs a very thorough bit test of each RAM address and takes about two minutes to complete. The screen shows the positions of the RAMs under test. Red indicates a bad RAM, and green indicates good.

4. BACKGROUND/COLOR VIDEO RAM TEST
Checks both the background screen video RAM and the color map RAM. The display will begin all white and then change to black from top to bottom. Any bad RAMs will appear in a red message on the screen. Additionally, bad video RAMs will generate a series of tones from the sound board. This will aid the operator or serviceman should the video RAMs be so bad that reading the messages on the screen is impossible. Each bad RAM will first sound a low tone followed by a number of high tones per the following table:

RAM	HIGH TONES
U52	1
U51	2
U50	3
U49	4
U28	5
U26	6

5. FOREGROUND VIDEO RAM TEST
This test checks the foreground screen video RAM. The screen will change colors from top to bottom. Since there are two foreground video screen RAM areas in this system, and only one screen can be displayed at one time, there will be a period of no screen activity even though the test is running. It is simply checking the screen RAM that is not currently being displayed. Bad RAMs will show messages on the screen and also generate tones as explained in step 4.

RAM	HIGH TONES
U57	1
U56	2
U55	3
U54	4

NOTE: The memory tests of steps 2 through 5 can be set to automatically continuously repeat by turning DIP switch #7 on. This would be useful if an intermittent memory failure is suspected. The memory tests continue to cycle until a bad check is detected and then freeze the screen showing the bad I.C. After #7 is turned on, start the cycle by running any of the memory tests. Don't forget to turn #7 off after you have finished the automatic tests.

6. DIP SWITCH SETTINGS
Displays the settings and functions of the eight DIP switches on the video mother board. The selected setting

appears in white on the screen. Any changes to the switch settings are immediately updated on the display.

7. PLAYER SWITCH TEST
This step displays player and coin switches as they are pressed. Also shown is the status of the joystick rotate counters. These counters should always be zero when entering the test and count up as a joystick is rotated clockwise and count down when rotated counterclockwise. The displayed count is a hexadecimal number between 0 and 3F.

8. SOUND OUTPUT TEST
Selecting this test displays a submenu permitting the operator a choice of four test functions or the option of returning to the main menu. The four subfunctions act as follows:

   A. OUTPUT PORT BIT WALK. Checks the connections between the video mother board and the sound board. The screen shows the connector pin numbers for all eight interconnecting data wires. The test pulses each data line individually low which creates a tone from the sound board. A properly operating system will repeatedly play an ascending musical scale. A missing note probably means a bad connection.

   B. SPEECH SOUND CODE. Speaks the phrase "Help me" when a left button is pressed.

   C. YAMAHA MUSIC CODE. Plays the "end of wave" music when a left button is pressed.

   D. DAC SOUND CODE. The wasp sting (dentist drill) sounds when a left button is pressed.

9. MONITOR TEST PATTERNS
Use this check to assess the adjustments on your monitor. The display shows you a submenu of the following various test patterns:

   A. CROSS HAIR. A white pattern used for centering and squaring your picture.

   B. RED LINE GRID. Tests the red color gun.

   C. GREEN LINE GRID. Tests the green color gun.

   D. BLUE LINE GRID. Tests the blue color gun.

   E. WHITE LINE GRID. Uses all three color guns.

   F. DOT PATTERN. White dots to check convergence.

   G. COLOR BARS. Seven vertical stripes from red to violet.

VIII. GENERAL INFORMATION

A. PRINTED CIRCUIT BOARDS ARE DESIGNATED AS FOLLOWS:

A1 VIDEO BOARD ASSEMBLY
A2 POWER SUPPLY
A5 AUXILIARY POWER SUPPLY
A6 SOUND BOARD ASSEMBLY
A8 VIDEO CONTROL INTERFACE ASSEMBLY

B. WIRE COLORS ARE SHOWN AS NUMBERS:

0 Black
1 Brown
2 Red
3 Orange
4 Yellow
5 Green
6 Blue
7 Violet
8 Gray
9 White

For example, 688 is a BLUE-GRAY-GRAY striped wire.

C. FUSES

TRANSFORMER PANEL/LINE FILTER

F1	LINE INPUT....................	110V AC...8 AMP SLO-BLO
		220V AC...4 AMP SLO-BLO
F2	PRIMARY POWER.................	110V AC...5 AMP SLO-BLO
		220V AC...2.5 AMP SLO-BLO
F3	MONITOR.......................	110V AC...1 AMP SLO-BLO
F4	FLUORESCENT LAMP/BALLAST......	110V AC...1/2 AMP SLO-BLO
F5	ILLUMINATION..................	6.2V AC...1 AMP SLO-BLO

POWER SUPPLY ASSEMBLY (A2)

*	LINE INPUT.....................	100V AC....2 AMP
		220V AC....2 AMP

* NOTE:
TO CONVERT TO 220V AC OPERATION, REMOVE POWER SUPPLY COVER AND CHANGE SELECTABLE JUMPER POSITION.

VIII. GENERAL INFORMATION

POWER SUPPLY SPECIFICATIONS

LOCATION	VOLTAGE	PROTECTION
Video Board Assembly Sound/Speech Board Video Control Interface Board	+5V DC	Voltage adjustable. 5 Amps with a line fuse inside the switching power supply.
Sound/Speech Board Auxiliary Power Supply Optional Electronic Coin Acceptor Coin Meter	+12V DC	2-1/2 Amps with line fuse inside the switching power supply.
Sound/Speech Board	-12V DC	500 Milliamps with a line fuse inside the switching power supply.
Coin Chute Lamps	6.2V AC	Power transformer winding with a 1 Amp Slo-Blo fuse (F5).
Monitor	115V AC	Power transformer isolation winding with a 1 Amp Slo-Blo fuse (F3).
Marquee	115V AC	Power transformer isolation winding with a 1/2 Amp Slo-Blo fuse (F4).

NOTES:

1) The switching power supply line input voltage is 115V AC. The output voltages are +5V DC @ 5 Amps, +12V DC @ 2-1/2 Amps, and -12V DC @ 1/2 Amps.
2) Converting the game for different input power voltages requires changing the jumpers at connector A12J5 and changing the selectable jumper position in the Switching Power Supply (A2).

IX. THEORY OF OPERATION

The Video Board Assembly (A1) is built with two Graphic System Processors (GSP). The GSP combines the best features of general-purpose processors and graphics controllers to create a powerful and flexible graphics system. Key features of the GSP are its speed, high degree of programmabaility, and efficient manipulation of hardware-supported data types such as pixels and two-dimensional pixel arrays.

The GSP's unique memory interface reduces the time needed to perform tasks such as bit alignment and masking. The 32-bit architecture supplies the large blocks of continuously-addressable memory that are necessary in graphics applications. The GSP supports the use of VRAM (video RAMs, which are used widely in graphics applications) by generating the memory-register cycles necessary to refresh a screen.

The Video Board Assembly (A1) is implemented using Master/Slave interface design features. The Master GSP executes the game program, services input/output ports, displays the background graphics and communicates to the Slave GSP. The Slave GSP performs the foreground graphic animation only (We call it an animation engine).

The screen resolution is 256 pixels across the horizontal scan line and 240 lines vertically. Each pixel of the background is represented with 15 bits which are partitioned with 5 bits of red, green and blue. Therefore it can display any one color out of 32768 total available color palette when the system is configured as direct background display mode. When the system is configured as in-direct background display mode, least 12 bits of pixel data are addressing the color lookup table. Color look up table is 15 bits wide and 4096 deep. Consequently, a pixel of in-direct background display mode can diplay one out of 4096 available colors at one time. The 4096 color palette can be any of 32768 total available colors.

The foreground animation engine uses the double-frame-buffer method. The double-frame-buffer method has 2 sets of frame buffer and it operates while one is refreshing display onto the monitor, the other is updated with the next frame display information. A pixel in foreground is represented with 8 bits. These 8 bits of pixel data are addressing the lower 256 address of the color lookup table. Finally, the foreground color is derived via the content of CLUT(Color Look Up Table), which gives 256 possible color choices out of 4096 available colors at one time.

SECTION 1. Master GSP

A. Master GSP local address interface

The GSP local memory interface consists of a triple-multiplexed address/data bus and associated controls. During a memory cycle, the row address, column address, and data are transmitted over the same bus line. At the start of a cycle, row address is output on MLAD0 - MLAD15 and is valid before and after MRAS falls. A column address is then output on MLAD0 - MLAD15. The column address is valid briefly before and after the falling edge of MLAL, but is not valid at the falling edge of MCAS. The column address is clocked into an external transparent latch (U33) on the falling edge of MLAL to provide the hold time on the column address required for DRAMs and VRAMs. A transparent latch (U33) is required so that the row address is available at the latch output during the start of the cycle.

The GSP can be programmed to perform DRAM-refresh cycles at regular intervals and also be programmed to perform screen refresh by scheduling VRAM shift-register transfer cycle to occur at regular

intervals. The Video Board Assembly (A1) uses DRAM that 256 rows are needed to be refreshed within 4 msec., DRAM-refresh cycle is programmed to refresh each row at every 64 local clock periods. Screen refresh is programmed for every horizontal blank time period.

The synchronization and blanking signals to drive a monitor are also generated in the Master GSP.

B. LOCAL DATA BUS

The 16-bit data bus is masked from a triple-multiplexed address/data bus while local data enable signal is low. During this time bidirectional data buffers (U17, U18) are enabled.

C. LOCAL ADDRESS BUS

Two different types of address bus are needed in the design. One is multiplexed row and column addresses to address the memories in the circuit. The other is the latched addresses to address EPROM or EEROM while they are selected. Also, latched higher addresses are for the selection of different types of memory or different banks within the same type of memory.

The multiplexed address bus to address VRAM and DRAM are masked in U33. Higher addresses for decoding purpose are latched and valid at transparent latch U31 and U32.

D. Background frame buffer

It contains 128 Kbytes of dual ported video memories to represent 256 pixels by 256 lines of 16 bits per pixel data. It is located in Master GSP address 0H through FFFFFH. Since, the data path of GSP is 16-bit wide, 4 chips of 64K x 4 VRAMs (U49, U50, U51, U52) are used in this design and they are accessed at the same time. This VRAM select signal (MVRAS) is decoded at U46 (PAL 2). The multiplexed lower 8 bits of address are driven from U33 and feed into the VRAMs.

The video memory mapped address are;

```
------------ ADDRESS BITS -------------
3322 2222 2222 1111 1111 1100 0000 0000
1098 7654 3210 9876 5432 1098 7654 3210

xxxx xx00 0xxx ssss ssss ssss ssss ssss    : Background VRAM
                                             block
where    x: don't care
       0/1: fixed value for address decoding
         s: valid address
```

E. PROGRAM AND STORAGE MEMORY

The Video Board Assembly (A1) has 512 Kbytes to store programs, table images etc. It is located Master GSP address 800000H through 8FFFFFH. The current design uses 256 K x 4 DRAMs(U67, U68, U69, U70). They are selected by the MDRAS0 signal which is decoded and generated at PAL 1 (U47).

IX. THEORY OF OPERATION

The Master GSP DRAM mapped addresses are;

```
------------ ADDRESS BITS -------------
3322 2222 2222 1111 1111 1100 0000 0000
1098 7654 3210 9876 5432 1098 7654 3210

xxxx xx00 1xss ssss ssss ssss ssss ssss  : Master DRAM bank

where    x: don't care
       0/1: fixed value for address decoding
         s: valid address
```

The most significant multiplexed address (MRA 8) of the DRAM bank is not derived from the GSP. Therefore, this address is generated from the latched local address bit 20 and 21 by combining these two addresses in corresponding row and column time. This process is done in PAL 2 and the signal name is called BRA8.

F. PROGRAM EPROM MEMORY

The current design has up to 2 Mbytes Program storage area. This EPROM select signal (ROMS) is decoded at PAL 2 (U46). The signal, ROMS, is further decoded to MRS0 - MRS15 at U95 and U96.

The EPROM mapped addresses are;

```
------------ ADDRESS BITS -------------
3322 2222 2222 1111 1111 1100 0000 0000
1098 7654 3210 9876 5432 1098 7654 3210

xxxx xx11 0000 ssss ssss ssss ssss ssss  : MRS 0
xxxx xx11 0001 ssss ssss ssss ssss ssss  : MRS 1
xxxx xx11 0010 ssss ssss ssss ssss ssss  : MRS 2
xxxx xx11 0011 ssss ssss ssss ssss ssss  : MRS 3
xxxx xx11 0100 ssss ssss ssss ssss ssss  : MRS 4
xxxx xx11 0101 ssss ssss ssss ssss ssss  : MRS 5
xxxx xx11 0110 ssss ssss ssss ssss ssss  : MRS 6
xxxx xx11 0111 ssss ssss ssss ssss ssss  : MRS 7

xxxx xx11 1000 ssss ssss ssss ssss ssss  : MRS 8
xxxx xx11 1001 ssss ssss ssss ssss ssss  : MRS 9
xxxx xx11 1010 ssss ssss ssss ssss ssss  : MRS 10
xxxx xx11 1011 ssss ssss ssss ssss ssss  : MRS 11
xxxx xx11 1100 ssss ssss ssss ssss ssss  : MRS 12
xxxx xx11 1101 ssss ssss ssss ssss ssss  : MRS 13
xxxx xx11 1110 ssss ssss ssss ssss ssss  : MRS 14
xxxx xx11 1111 ssss ssss ssss ssss ssss  : MRS 15

where    x: don't care
       0/1: fixed value for address decoding
         s: valid address
```

G. EEPROM- Backup MEMORY

The backup memory is to save the status of game, the options of the game, etc. This EEPROM is write protected during power failure through the "Hold-Low". That is to pull the /OE to a logic 0 (low) whenever the supply voltage is below the system threshold. The programmable voltage reference (U6) is sensing a selected voltage threshold and outputs a logic 0 when the supply voltage is below that threshold which is programmed at 4.5 Volt. Conversely, as the

sensed voltage rises above the selected threshold (programmed at 1.56 Volt), it outputs a logic 1 (high) following its supply voltage level.

These EEPROM address are decoded at PAL 2 (U46) and selected by the signal EERS.

The EEPROM mapped address is;

```
------------ ADDRESS BITS -------------
3322 2222 2222 1111 1111 1100 0000 0000
1098 7654 3210 9876 5432 1098 7654 3210

xxxx xx10 1xxx xxxx xsss ssss ssss ssss   : EEPROM

where    x: don't care
       0/1: fixed value for address decoding
         s: valid address
```

H. Color Look Up Table

The size of CLUT is 2 Kwords and they are located at addresses 1800000H - 1807FFFH. This color look up table select signal (LUTEN) is decoded at PAL 2 (U46).

Color Look Up Table is addressed from the output of the 4 to 1 multiplexers(U41, U42, U43, U44, U45 and U58). These multiplexers select one out of three different groups of address bus. And, they are Master GSP local address bus to download or read the CLUT, foreground pixel data to drive the foreground display color palette and the background pixel data when it is in-direct background display mode. The two select control signals(TMUX0 and TMUX1) are generated at PAL 4(U61). Two bi-directional transceivers (U12, U14) are added to isolate CLUT data bus from the rest of the Master GSP local data bus.

The Color Look Up Table address is;

```
------------ ADDRESS BITS -------------
3322 2222 2222 1111 1111 1100 0000 0000
1098 7654 3210 9876 5432 1098 7654 3210

xxxx xx01 1xxx xxxx xsss ssss ssss ssss   : CLUT

where    x: don't care
       0/1: fixed value for address decoding
         s: valid address
```

I. Input Port

There are 3 input ports (IP0S, IP1S, IP2S) are available in this design. The input port select signal (IPEN) is decoded at PAL 1 (U47). IPEN is further decoded at U24. IP0S and IP1S are 16 bits per each channel and used for general purpose game control input ports (IP00 - IP1D). The 2 MSBs of IP1S (IP1E and IP1F) are used for receiving a status of the sound board. All the input port bits are connected through the FCC filters and RRC noise filters to octal buffers (U3, U4, U7, U9). IP2S is a 8-bit wide only and it is dedicated for the on-board option switch SW0 - SW7, U1.

IX. THEORY OF OPERATION

The Input Ports addresses are;

```
------------ ADDRESS BITS -------------
3322 2222 2222 1111 1111 1100 0000 0000
1098 7654 3210 9876 5432 1098 7654 3210

xxxx xx01 0100 00xx xxxx xxxx xxxx 0000  : IP0S
xxxx xx01 0100 01xx xxxx xxxx xxxx 0000  : IP1S
xxxx xx01 0100 10xx xxxx xxxx xxxx 0000  : IP2S

where    x: don't care
       0/1: fixed value for address decoding
         s: valid address
```

J. Output Port

The output port select signal (OPEN) is decoded at PAL 1 (U47). OPEN is further decoded at U24. There are 13 general purpose output port bits (OP00 -OP0C) available from the output port latch(OP0S) U8 and U10. The 2 MSBs of OP0S(OP0E and OP0F) are used to drive two coin counters. The 13th bit(OP0D) is to reset the Slave GSP. SOUND port is a byte-wide only and send a messages to the sound board through this output port latch (U11).
WDOG port is for the watch dog clear port.
Master GSP sends out a pulse to reset the watchdog counter (U35) through the WDOG output port. When it fails to clear the counter for the 16 consecutive frame times, it will reset the Master GSP.

The Output Ports addresses are;

```
------------ ADDRESS BITS -------------
3322 2222 2222 1111 1111 1100 0000 0000
1098 7654 3210 9876 5432 1098 7654 3210

xxxx xx01 0101 00xx xxxx xxxx xxxx 0000  : OP0S
xxxx xx01 0101 10xx xxxx xxxx xxxx 0000  : SOUND
xxxx xx01 0101 11xx xxxx xxxx xxxx 0000  : WDOG

where    x: don't care
       0/1: fixed value for address decoding
         s: valid address
```

K. Slave GSP Interface

The Master GSP communicates with Slave GSP by means of an interface bus consisting of a 16-bit data path and several transfer control signals. The Master and Slave interface provides a master with access to four programmable 16 bit registers (resident on the GSP), which are mapped into four locations in the Master GSP memory address space. Through this interface commands, status information, and data are transferred between the two Master and Slave GSPs.

These four registers are called HSTADRL, HSTADRH, HSTDATA and HSTCTL. The HSTADRL and HSTADRH registers contain the 16 LSBs and 16 MSBs, respectively, of a 32-bit address pointer. A host(Master GSP) processor uses this address to indirectly access GSP local memory. HSTDATA register buffers data that is transferred through the host interface between GSP local memory and a host processor.

HSTDATA contains the contents of the address pointed to by the HSTADRL and HSTADRH registers. The HSTCTL register is accessible to the GSP as two separate I/O registers, HSTCTLL and HSTCTLH, but is accessed by a host processor as a single 16-bit register. HSTCTL contains several programmable fields that control host interface functions.

These four register address spacse are decoded at PAL 1 (U47) and selected by the signal SHCS.

The Slave GSPs Four Registers addresses are;

```
------------ ADDRESS BITS -------------
3322 2222 2222 1111 1111 1100 0000 0000
1098 7654 3210 9876 5432 1098 7654 3210

xxxx xx01 0000 00xx xxxx xxxx xxxx 0000   : HSTADRL
xxxx xx01 0001 00xx xxxx xxxx xxxx 0000   : HSTADRH
xxxx xx01 0010 00xx xxxx xxxx xxxx 0000   : HSTDATA
xxxx xx01 0011 00xx xxxx xxxx xxxx 0000   : HSTCTL
```

```
where     x: don't care
        0/1: fixed value for address decoding
          s: valid address
```

L. Summary of Master GSP address decode

```
------------ ADDRESS BITS -------------
3322 2222 2222 1111 1111 1100 0000 0000
1098 7654 3210 9876 5432 1098 7654 3210

xxxx xx00 0xxx ssss ssss ssss ssss ssss   : Background VRAM

xxxx xx00 1xss ssss ssss ssss ssss ssss   : Master DRAM

xxxx xx01 00ss 00xx xxxx xxxx xxxx 0000   : Slave GSP

xxxx xx01 0100 ssxx xxxx xxxx xxxx 0000   : Input port

xxxx xx01 0101 ssxx xxxx xxxx xxxx 0000   : Output Port

xxxx xx01 1xxx xxxx xsss ssss ssss ssss   : CLUT

xxxx xx10 1xxx xxxx xsss ssss ssss ssss   : EEPROM

xxxx xx11 ssss ssss ssss ssss ssss ssss   : EPROM
```

```
where     x: don't care
        0/1: fixed value for address decoding
          s: valid address
```

IX. THEORY OF OPERATION

SECTION 2. Slave GSP

A. Slave GSP host interface

The Master GSP communicates with Slave GSP by means of an interface bus consisting of a 16-bit data path and nine control signals. The four host interface registers are a subset of the I/O registers. These four host interface registers located in Slave GSP are accessed by both Master GSP and Slave GSP. The four registers are memory mapped and they are selected by placing a particular code on the two function select inputs, HFS0 and HFS1.

The Master GSP indirectly accesses Slave GSP's local memory by reading from or writing to the HSTDATA register. HSTDATA buffers data written to or read from the local memory. The word in local memory that is accessed is the word pointed to by the 32-bit address contained in the HSTADRL and HSTADRH registers (ADDRESS register). The pointer address is loaded into address register by the Master GSP before performing one or more indirect accesses of local memory using the HSTDATA register (DATA register).

The four LSBs of HSTADRL are forced to 0s internally so that the address formed by ADDRESS register always points to a word boundary in local memory. Between successive indirect accesses of local memory using the DATA register, the local memory address contained in the ADDRESS registers can be autoincremented by 16. This allows the Master GSP to access a block of sequential words in local memory without the overhead of loading a new address prior to each access.

During a sequence of one or more indirect reads of local memory by the Master GSP, the Slave GSP maintains in HSTDATA a copy of the local memory word currently addressed by the ADDRESS register. Reading from DATA register returns the word prefetched from the local memory location pointed to by the ADDRESS register, and causes HSTDATA to be updated from local memory again. Writing to DATA register causes the word written to HSTDATA to subsequently be written to the location in local memory pointed to by the ADDRESS registers.

Loading the pointer address automatically triggers an update of HSTDATA to the contents of the local memory word pointed to. No increment of ADDRESS register takes place at this time regardless of the state of the increment bits. Each subsequent host access of DATA register causes ADDRESS register to be automatically incremented (or decremented) to point to the next word location in the local memory. In this manner, a series of contiguous words in local memory can be accessed following a single load of the ADDRESS register without additional pointer-management overhead.

Host interface read and write cycles are initiated by the Master GSP and are controlled by means of the /HCS, /HWRITE, /HREAD, /HUDS, and /HUDS signals. At least three control signals must be active at the same time to initiate an access. The last of the three signals to become active begins the access, and the first of the three signals to become inactive signals the end of the access. A signal that begins or completes an access is referred to as the strobe signal for the cycle. Any of the five signals listed above may be a strobe.

IX. THEORY OF OPERATION

B. SLAVE GSP LOCAL DATA BUS

The local data enable signal (SDEN) is driven active low to allow 16-bit data to be written to or read from SLAD0 - SLAD15. The local data direction out signal (SDDOUT) is driven high to enable data to be output on SRD0 - SRD15. It is driven low to enable data to be input to the Slave GSP. These two signals control the local data bus transceivers (U37 and U38).

C. LOCAL ADDRESS BUS

The multiplexed address bus to address VRAM and DRAM is generated in U37. These 8-bit multiplexed address lines (SRA0 - SRA7) are addressing all the local memories. The most significant address bit (SRA8) for the 256 K DRAM is driven from PAL 3(U40). The higher addresses to decode the different types of memory bank are latched at U25.

D. Foreground frame buffer

It contains a total of 128 Kbytes of dual ported video memories to represent two sets of 256 pixels by 256 lines by 8 bits per pixel data. The first set of the foreground frame buffer is located in Slave GSP address 0H through 7FFFFH. The other set of the dual frame buffer is located in address 80000H through FFFFFH. Since, the data path of GSP is 16-bit wide, 4 chips of 64K x 4 VRAMs (U54, U55, U56, and U57) are accessed at the same time.

The Slave GSP's VRAM select signal(FRAS) is decoded at PAL 3(U40). The multiplexed lower 8 bits of RAM addresses are driven from U39 and feed into all the VRAMs.

The foreground video memory address is;

```
------------ ADDRESS BITS -------------
3322 2222 2222 1111 1111 1100 0000 0000
1098 7654 3210 9876 5432 1098 7654 3210

xxxx x0xx xxxx ssss ssss ssss ssss ssss    : Foreground VRAM
                                             block

where     x: don't care
        0/1: fixed value for address decoding
          s: valid address
```

E. PROGRAM AND STORAGE MEMORY

The Slave GSP has 1 Mbyte to store program, table, images, etc. It is located in the Slave GSP address FF800000H through FFFFFFFFH. The current design uses two banks of 256 K x 4 DRAMs. The DRAM bank 0 (U71, U73, U75, U77) and DRAM bank 1 (U72, U74, U76, U78) are selected by SDRAS0 and SDRAS1 signals respectively. These signals are decoded and generated at PAL 3 (U40).

The Slave GSP's DRAM addresses are;

```
------------ ADDRESS BITS -------------
3322 2222 2222 1111 1111 1100 0000 0000
1098 7654 3210 9876 5432 1098 7654 3210

xxxx x1xx x0ss ssss ssss ssss ssss ssss  : Slave DRAM bank 1
xxxx x1xx x1ss ssss ssss ssss ssss ssss  : Slave DRAM bank 0


where     x: don't care
        0/1: fixed value for address decoding
          s: valid address
```

The most significant multiplexed RAM address(SRA 8) of DRAM is not drived from the GSP. Therefore, this address is generated from the latched local address bit 20 and 21 (SLA20 and SLA21) by combining these two addresses together in corresponding row and column times. This process is done in PAL 3 and the signal name is called FRA8.

F. Ready Signal to Master GSP

The default state of the bus ready output pin, HRDY, is active high. HRDY is driven inactive low to force the host processor to wait in circumstances in which the Slave GSP is not prepared to allow a host-initiated register access to be completed immediately.

HRDY is always driven low for a brief period at the beginning of a read or write access of the HSTCTL register (CONTROL register). When a Master attempts to read from or write to the CONTROL register, HRDY is driven low at the beginning of the access, and is driven high again after a brief interval of one to two local clock cycles.

When the Master processor performs certain types of host interface register accesses, a local memory cycle results. If the Master GSP attempts to perform an access that initiates a second local memory cycle before the Slave GSP has had sufficient time to complete the first, The Slave GSP drives its HRDY output low to indicate that the Master GSP must wait before completing the access. When the Slave GSP has completed the local memory cycle resulting from the previous access, it drives HRDY high to indicate that the Master GSP can now complete its second access.

The HRDY signal is activated by the /HCS input alone. In other words, HRDY can be active-low only while the Slave GSP is chip-selected by the Master GSP, that is, while /HCS is active low. A high-to-low transition on HRDY follows a high-to-low transition on /HCS. This way HRDY becomes valid as soon as /HCS goes low.

The HRDY output of Slave GSP signal (SRDY) is feed into Master GSP's LRDY input through the U34 and U53 gates.

IX. THEORY OF OPERATION

VIDEO CONTROL INTERFACE (A8)

The interface board converts pulse information from the joystick's optical rotary encoder into binary information for the video mother board. It also supplies +5 volts and ground to power the optical rotary encoders' LEDs.

The interface board has two identical logic sections (one for each joystick). Each section uses two inverters of U8 (Schmitt inverter) and 1/2 of U4 (D flip flop). The left joystick section consists of U5, U6, and U7. The right section uses U1, U2, and U3. U2, U3, U6, and U7 are binary up/down counters. U1 and U5 are hex buffers.

The orange and yellow wires coming from the rotary encoders pulse high and low as a joystick is rotated. These pulses vary with the speed and direction of rotation, and feed the D and Clock inputs of a D flip flop and the Clock input of an up/down counter. The D flip flop determines whether the counter should count up or down. While in the shooting bug spray mode, the video mother board periodically clears the counters and then reads any count up or count down action and adjusts the hand position accordingly.

SOUND BOARD (A6)

The Sound Board consists of two 6502 microprocessor systems, a dual DAC, input ports to receive commands from the game Control Board, and a low level audio output, which is sent to the Auxiliary Power Supply Board for amplification.

The Sound Board requires three supply voltages +5V DC, +12V DC and -12V DC. In addition a power up reset signal is required from the Control Board.

SYSTEM CLOCK

A 4 MHz oscillator is configured with R11, R12, C14, C15, C22, XTAL-1 and T1. This 4MHz clock is divided by 4 to a 1 or 2 MHz clock for both processors clock input, pin 37 of N1 and T3. A 250 KHz signal from S1 pin 11 is the clock for the programmable timer section consisting of N5, H5, T5 and K5, pin 2.

INPUT CODE LATCH SYSTEM

Eight input lines from the Control Board come in on A6P1 and are pulled up by S1P1 and sent to the two input code latches A3 and B2, one for each microprocessor system. A2, pin 8,becomes a logic high when any of it's inputs are low. this output is connected to pin 11 of the input code latches (A3 and B2). A positive edge at pin 11 causes A3 and B2 to latch the data at their inputs. A2 pin 8 is also connected to the clock inputs of two flip flops, A4 pin 3 and A4 pin 11. When A2 pin 8 goes high, both flip flops are clocked, setting both $\bar{Q}$ outputs low. The $\bar{Q}$ outputs, A4 pin 6 and pin 8, are connected to both of the 6502's active low interrupt request lines, T3 and N1, pin 4. The $\bar{Q}$ outputs of A4 will stay low until the associated 6502 reads its input port therefore clearing the interrupt.

SYSTEM EPROMS

The sound board is designed to accommodate different types of EPROMS. Jumpers JP1, 2, 3, and 4 should be set to the proper position based on the EPROM being used, (See Schematic Diagram).

RESET

The Sound Board receives an external reset signal from A1P4 pin 10. This active low reset signal is pulled up by R34 and sent to G5, pin 1 (2-input AND gate). However, if a manual reset is desired, pushing switch SW2 will reset the processor.

MAIN SUMMER

The main summer consists of R13 through R17 and B1, pins 12, 13 and 14. B1 pin 14 is the main output from the Sound Board, at A6P2 pin 9, and will swing plus or minus 5V peak to peak.

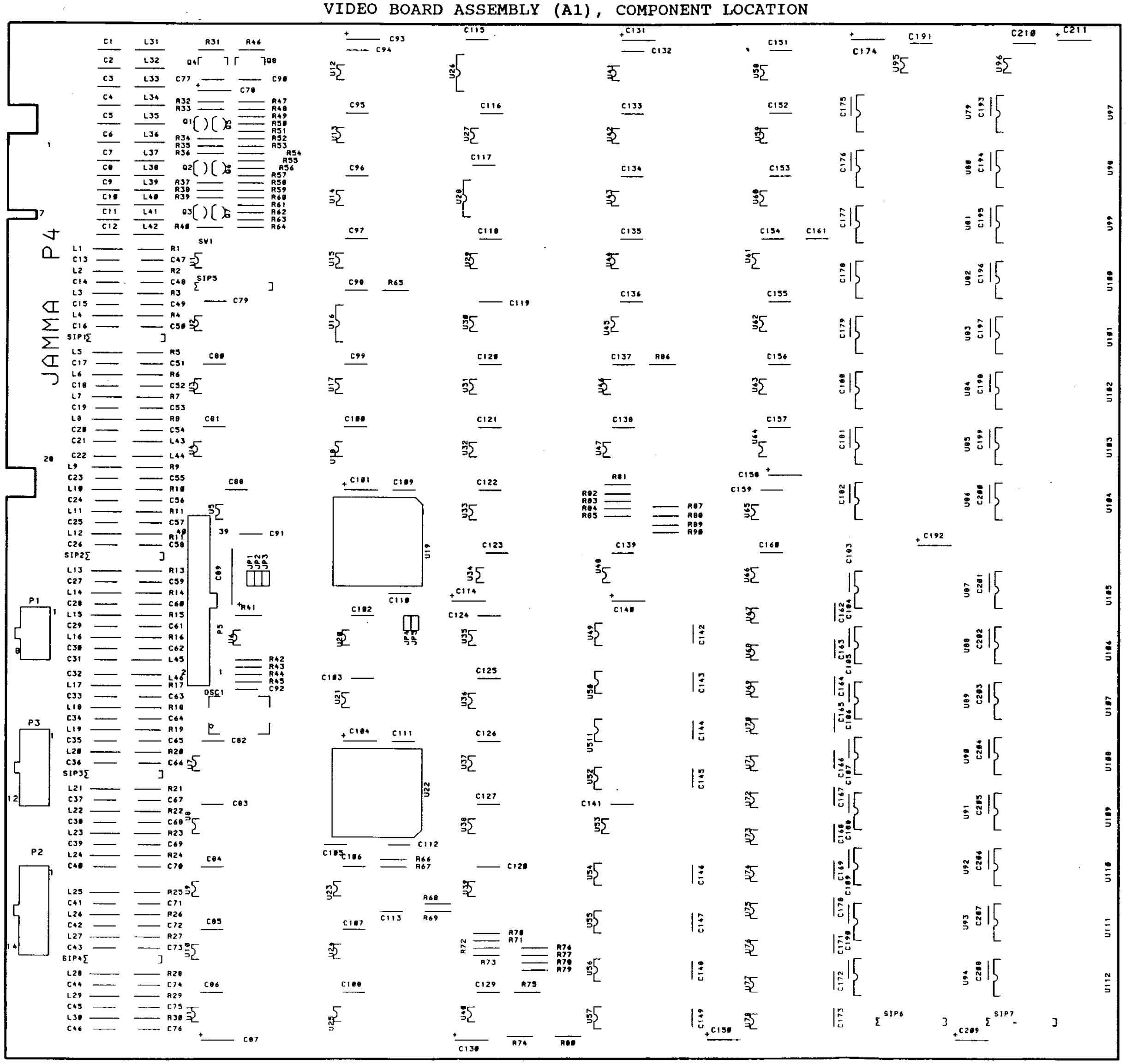
IX. THEORY OF OPERATION

AUXILIARY SOUND BOARD (A20)
The Auxiliary Sound Board consists of a YM2151 (U1) sound generator, a YM3014 (U2) DAC, and a LM324 op-amp (U3). The master Sound Board (A6), controls the YM2151 (U1) sound chip by sending commands via the data bus of the master Sound Board's T3 microprocessor. The YM2151 responds to these commands and serially sends sound data to the YM3014 DAC by means of the CLK, SD, and SH2 lines. The DAC converts this serial data into an analog signal which is buffered and amplified by U3, a LM324 op-amp. This analog signal is then sent back to the main summer of the master Sound Board (A6).

X. WIRING AND SCHEMATIC DIAGRAMS, PARTS LISTS

TABLE OF CONTENTS

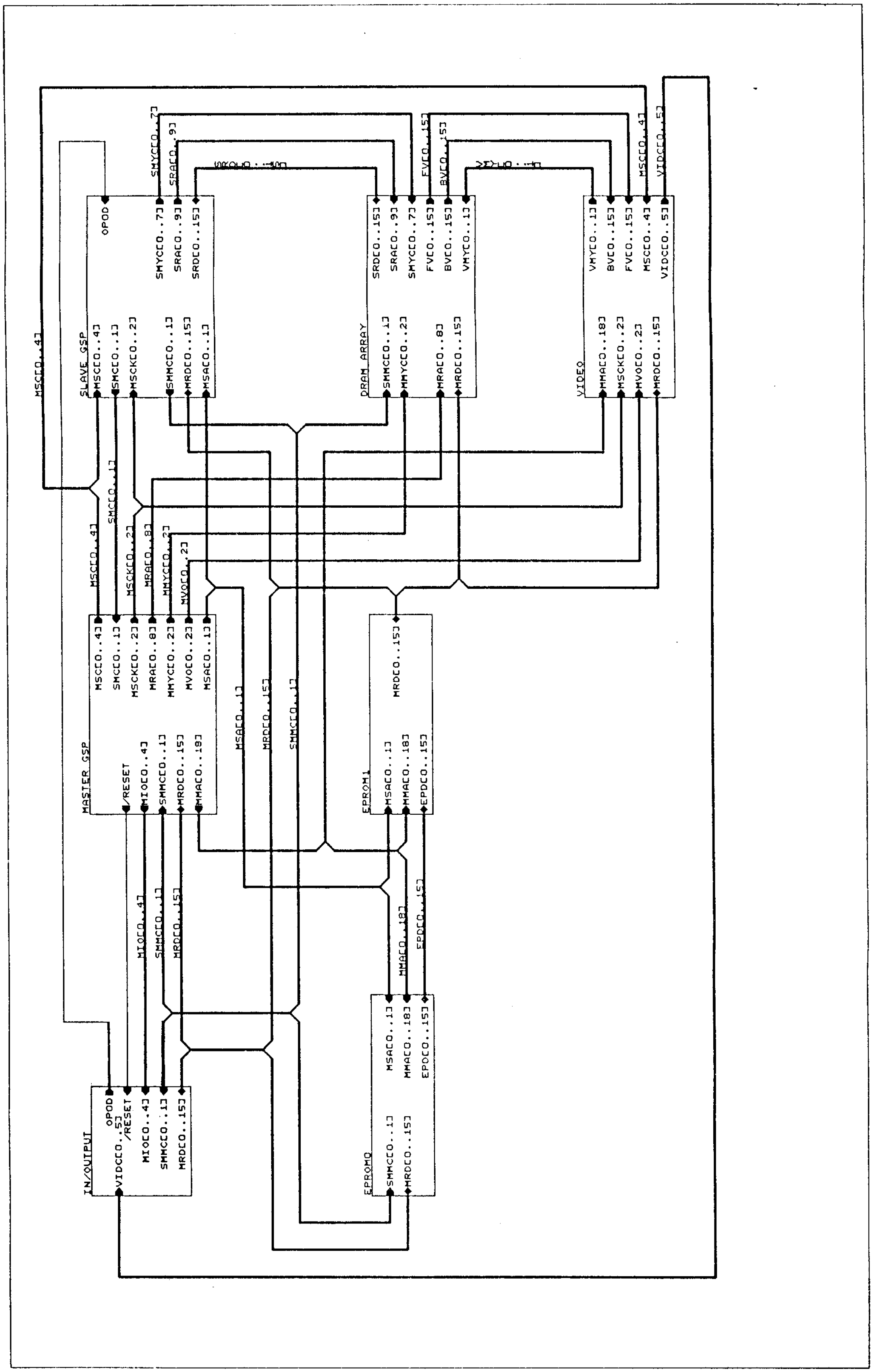
VIDEO BOARD ASSEMBLY (A1), COMPONENT LOCATION



VIDEO BOARD ASSEMBLY (A1) PARTS LIST

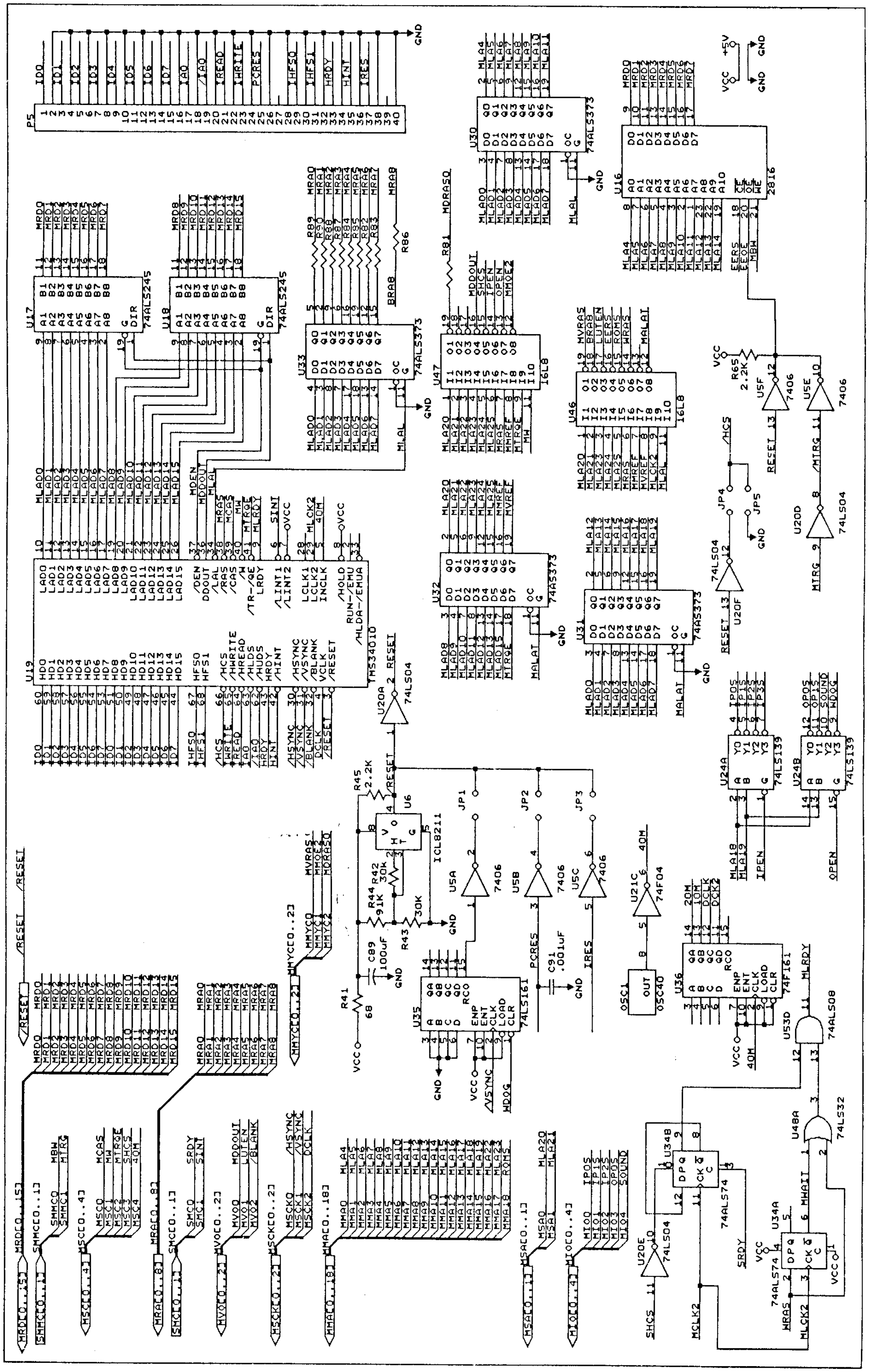
REFERENCE	DESCRIPTION	PART NO.
	Video Board Assembly	MA-1325
C1-C8,C13-C30, C33-C46,C79-C86, C88, C92,C94-C100 C102,C103,C105-C108,C109-C112, C115-C129,C132-C139,C141,C151-C157,C159,C191, C210	Capacitor, .01UF, +80-20%, 50V	XO-229
C9-C12,C31,C32	Capacitor, 39PF, 10%, 50V	XO-334
C47-C77,C90 C142-C149,C160, C162-C190,C193-C208	Capacitor, 0.1UF, +80-20%, 50V	XO-230
C78,C87,C93,C101, C104,C114,C130, C131,C140,C150, C158,C174,C192, C209,C211	Capacitor, 0.1UF, 20%, 25V	XO-127
C89	Capacitor, 100UF, 10V	XO-211
C91,C113	Capacitor, 1000PF, 10%, 100V	XO-296
C161	Capacitor, 150PF, 25V	XO-803
L1-L46	Ferrite Bead	XO-338
OSC1	Crystal, 40 Mhz	XO-972
Q1-Q3,Q5-Q7,	Transistor, MPSA70, PNP	XO-309
Q4,Q8	Transistor, 2N6043, NPN	XO-303
R1-R30	Resistor, 470 Ohm, 5%, 1/4W	XO-35
R31,R46,R47, R53,R59	Resistor, 1K Ohm, 5%, 1/4W	XO-5
R32,R33,R35, R36,R38,R39	Resistor, 15 Ohm, 5%, 1/4W	XO-171
R34,R37,R40	Resistor, 150 Ohm, 5%, 1/4W	XO-574
R41	Resistor, 68 Ohm, 5%, 1/4W	XO-748
R42,R43	Resistor, 30K Ohm, 5%, 1/4W	XO-988
R44	Resistor, 91K Ohm, 5%, 1/4W	XO-989
R45,R65	Resistor, 2.2K Ohm, 5%, 1/4W	XO-27
R66-R90	Resistor, 33 Ohm, 5%, 1/4W	XO-573
R48,R54,R60	Resistor, 270 Ohm, 5%, 1/4W	XO-68
R49,R55,R61	Resistor, 560 Ohm, 5%, 1/4W	XO-36
R50,R56,R62	Resistor, 1.2K Ohm, 5%, 1/4W	XO-175
R51,R57,R63	Resistor, 2.4K Ohm, 5%, 1/4W	XO-987
R52,R58,R64	Resistor, 4.7K Ohm, 5%, 1/4W	XO-7
SIP1-SIP5	Resistor, DIP, 4.7K,Ohm,10 Pin Sip	XO-906
SIP6-SIP7	Resistor, Dip, 1K Ohm, 9 Pin Sip	XO-493
U1 (SW1)	Dip Switch	XO-505
U2-U4,U7,U9	IC, 74LS244, Octal Buffer	XO-85
U5	IC, 7406, Buffer	XO-85
U6	IC, ICL8211, Voltage Detector	XO-971
U8,U10,U11	IC, 74LS377, Octal "D" Flip-Flop	XO-97
U12,U14,U17, U18,U37,U38	IC, 74LS245, Octal Transceiver	XO-981
U13,U15,U27,U29	IC, 74F534, Octal "D" Flip-Flop	XO-985
U16	IC, 2816, EEPROM	XO-969
U19,U22	IC, TMS34010, CPU	XO-964
U20	IC, 74LS04, Hex Inverter	XO-418
U21	IC, 74F04, Hex Inverter	XO-973
U23,U65,U66	IC, 74ALS244, Octal Buffer	XO-980
U24	IC, 74LS139, Dual 1 of 4 Decoder	XO-419
U25,U30,U33,U39	IC, 74ALS373, Octal Latch	XO-983
U26,U28	IC, 6116-12 SRAM 2K X 8, 120NS	XO-967
U31,U32	IC, 74AS373, Octal Latch	XO-984
U34	IC, 74ALS74, Dual "D" Flip-Flop	XO-976
U35	IC, 74LS161, Sync Preset Binary Counter	XO-440
U36	IC, 74F161, Binary Counter	XO-977
U40,U46,U47,U61	IC, 16L8ACN, PAL	XO-970
U41-U45,U58	IC, 74F153, Dual Multiplexer	XO-979
U48	IC, 74LS32, Quad "OR" Gates	XO-433
U49-U52,U54-U57	IC, 4461-15NL, VRAM	XO-963
U53	IC, 74ALS08, Quad "AND" Gates	XO-974
U59,U60	IC, 74F260, Dual "NOR" Gate	XO-982
U62,U63	IC, 74F74, Dual "D" Flip-Flop	XO-975
U64	IC, 74F157, Quad Data Selector	XO-978
U67-U78	IC, 424256-12, Dram 256K X 4,120NS	XO-966
U79-U94,U97-U112	IC, 27512-12, EPROM , 150NS	XO-968
U95-U96	IC, 74LS138, 1 of 8 Decoder	XO-437
P1	Header, 8 Position	XO-911
P2	Header, 14 Position	XO-914
P3	Header, 12 Position	XO-913
	Header, 40 Position	XO-992
	Header, 10 Position	XO-990

X. WIRING AND SCHEMATIC DIAGRAMS, PARTS LISTS



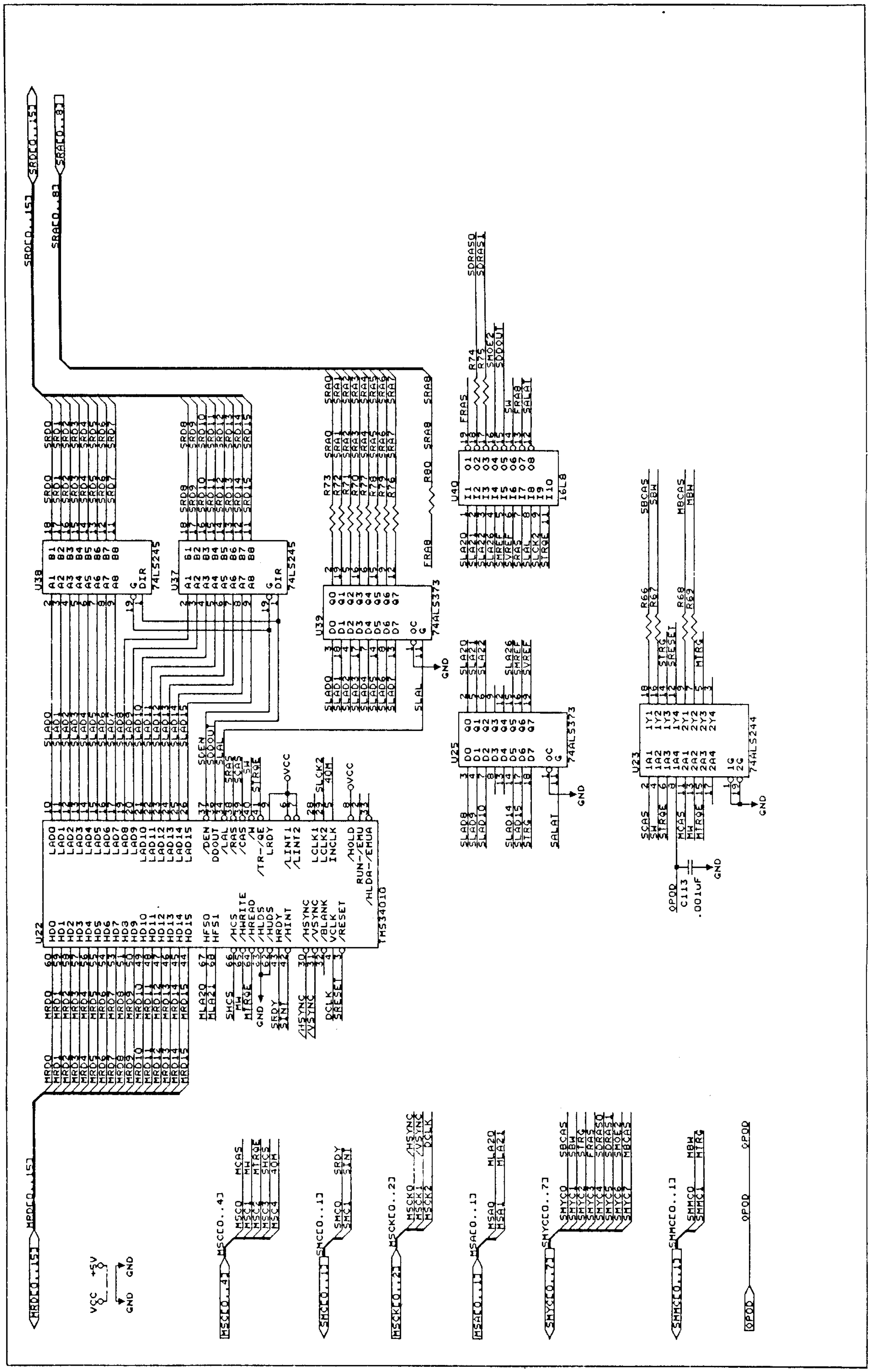
VIDEO BOARD ASSEMBLY (A1), SCHEMATIC DIAGRAM, SHEET 1 OF 8

X. WIRING AND SCHEMATIC DIAGRAMS, PARTS LISTS

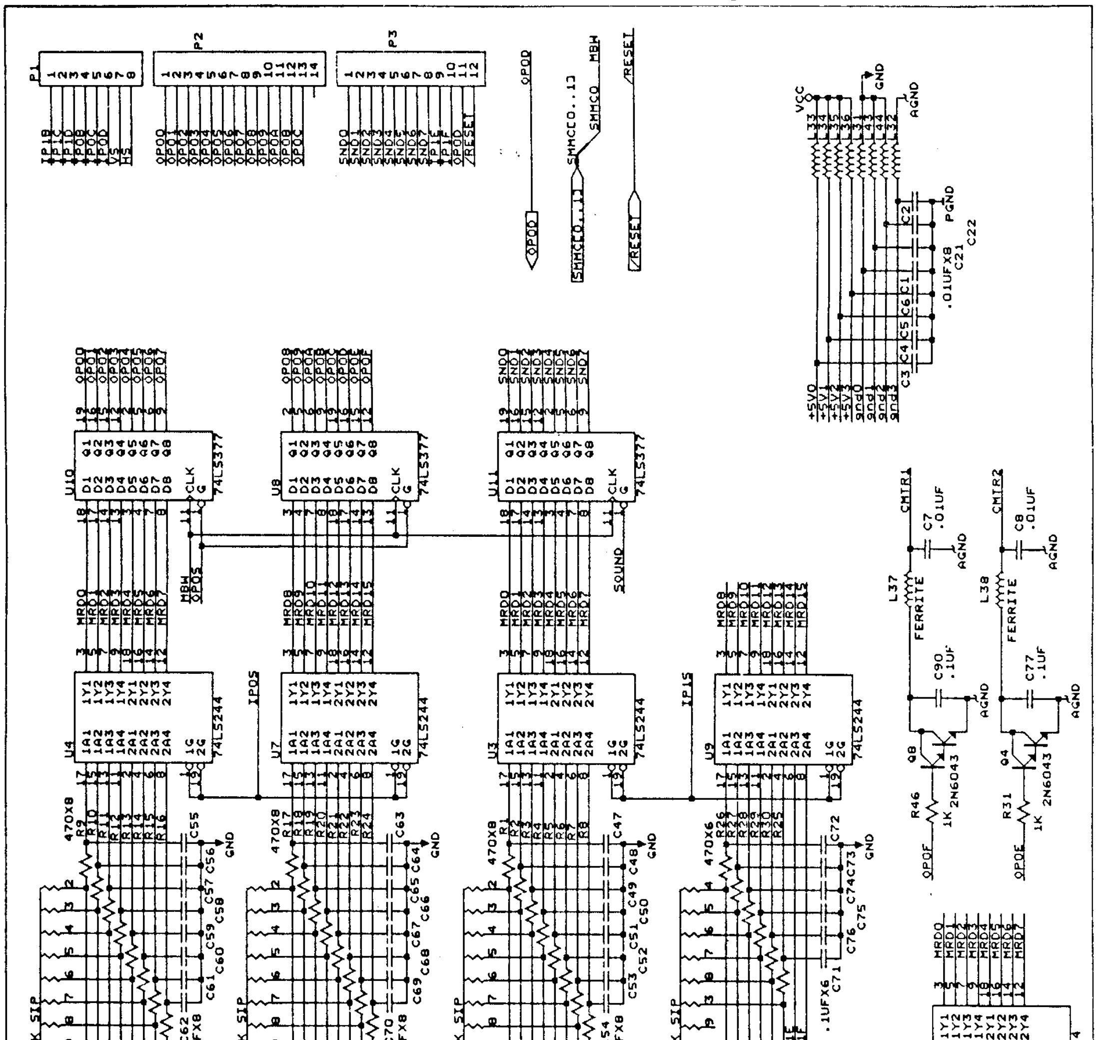


VIDEO BOARD ASSEMBLY (A1), SCHEMATIC DIAGRAM, SHEET 2 OF 8

X. WIRING AND SCHEMATIC DIAGRAMS, PARTS LISTS

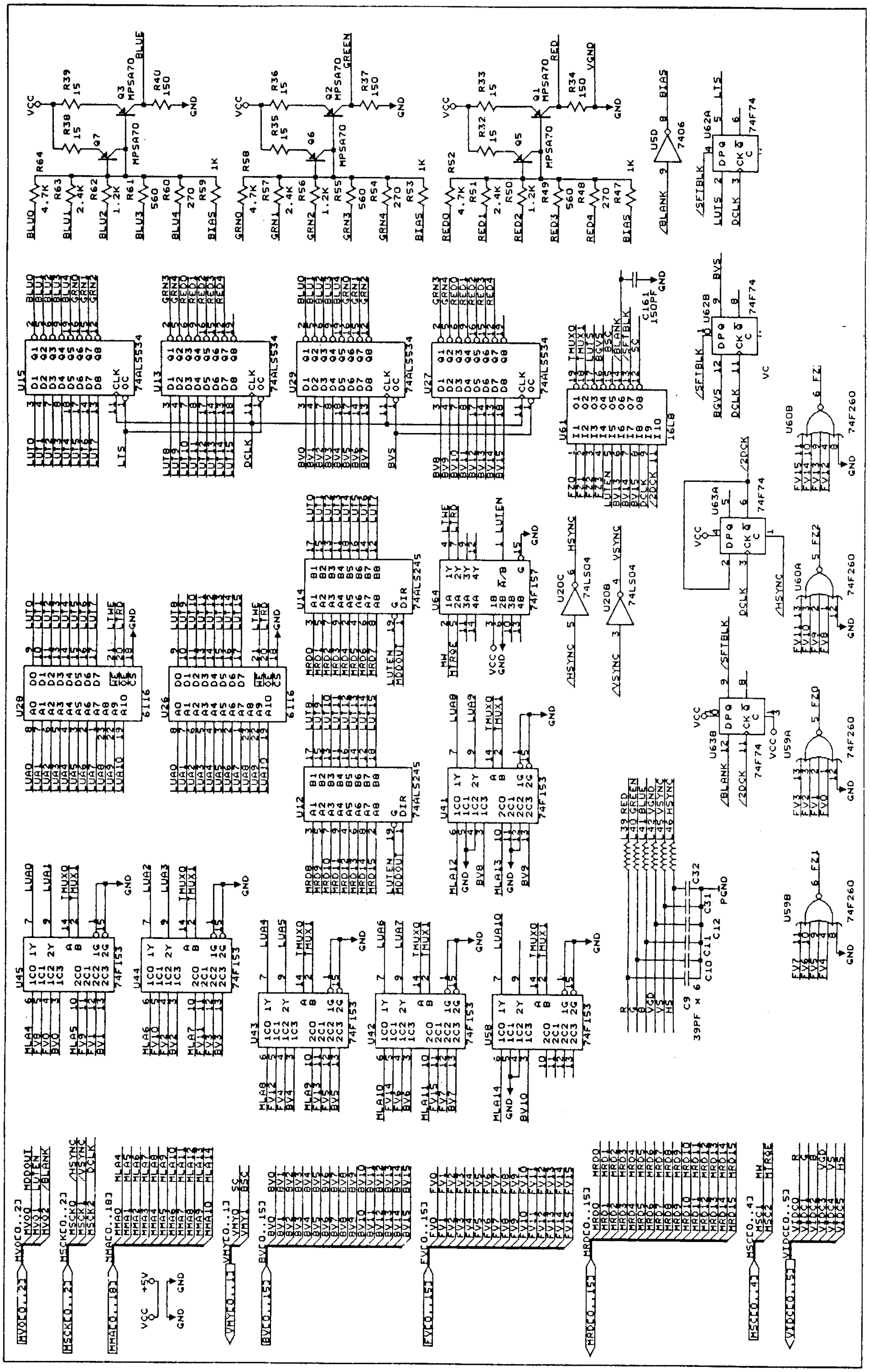


VIDEO BOARD ASSEMBLY (A1), SCHEMATIC DIAGRAM, SHEET 3 OF 8



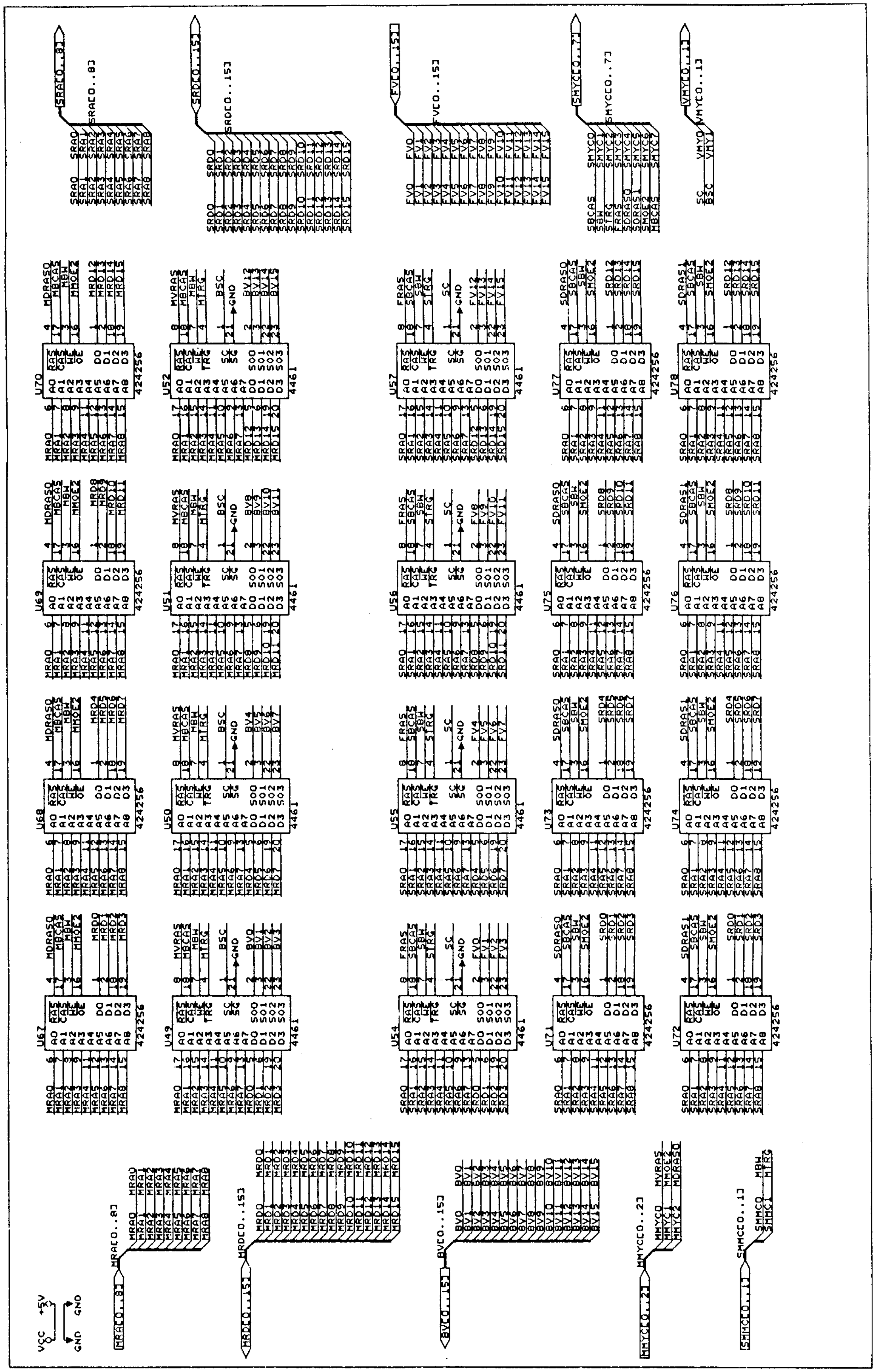
VIDEO BOARD ASSEMBLY (A1), SCHEMATIC DIAGRAM, SHEET 4 OF 8

X. WIRING AND SCHEMATIC DIAGRAMS, PARTS LISTS

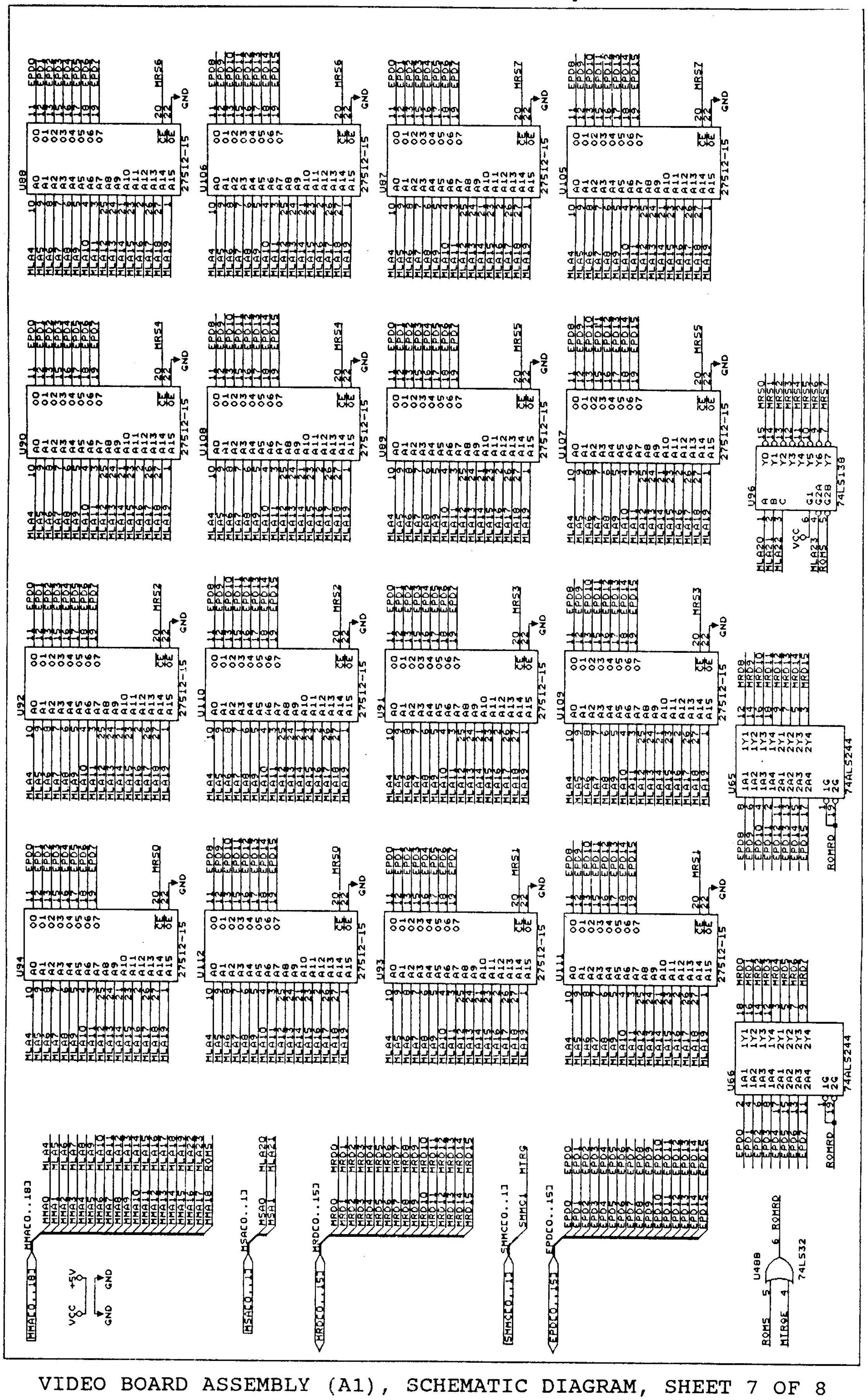


VIDEO BOARD ASSEMBLY (A1), SCHEMATIC DIAGRAM, SHEET 5 OF 8

X. WIRING AND SCHEMATIC DIAGRAMS, PARTS LISTS

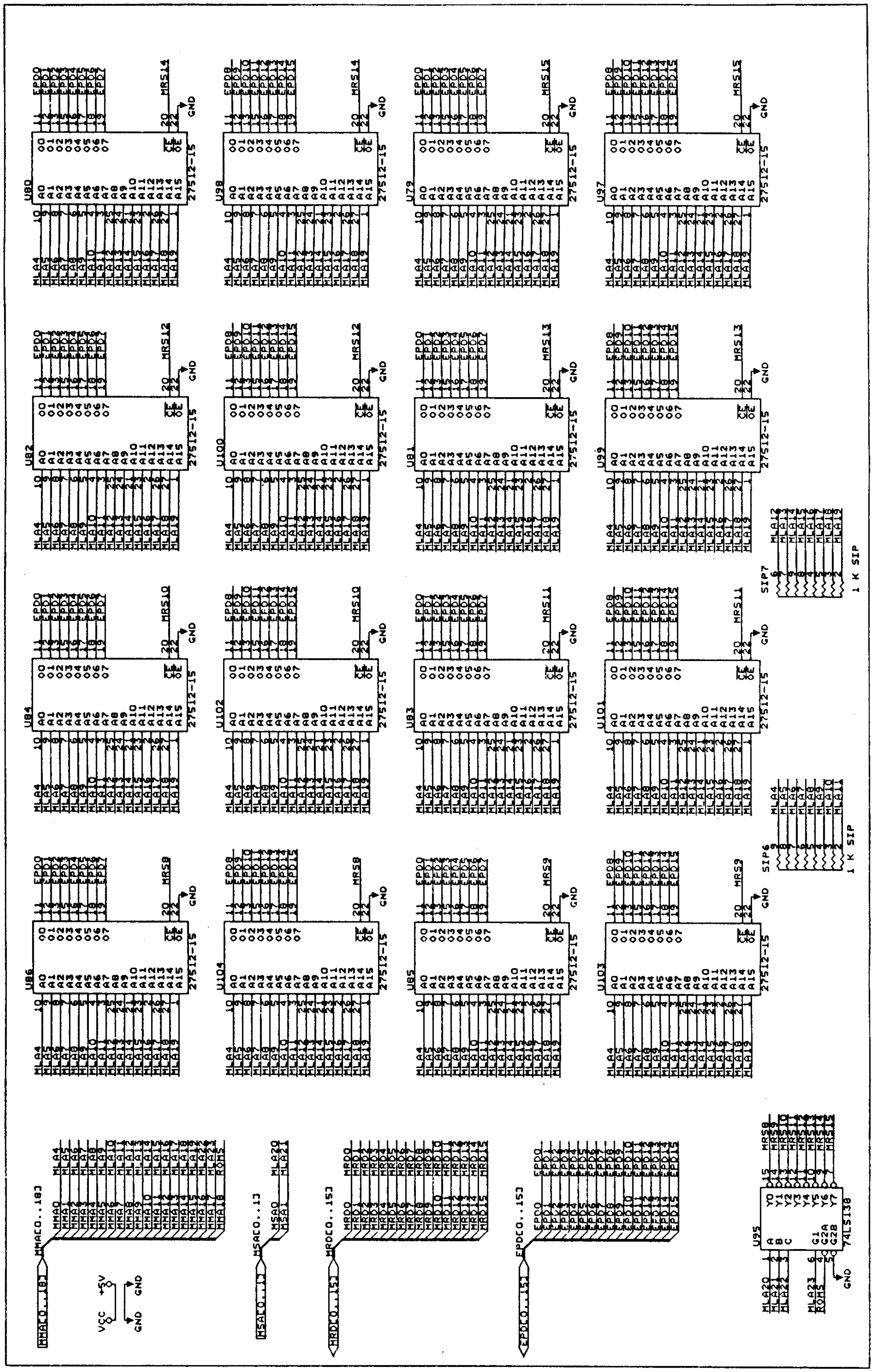


VIDEO BOARD ASSEMBLY (A1), SCHEMATIC DIAGRAM, SHEET 6 OF 8



VIDEO BOARD ASSEMBLY (A1), SCHEMATIC DIAGRAM, SHEET 7 OF 8

X. WIRING AND SCHEMATIC DIAGRAMS, PARTS LISTS

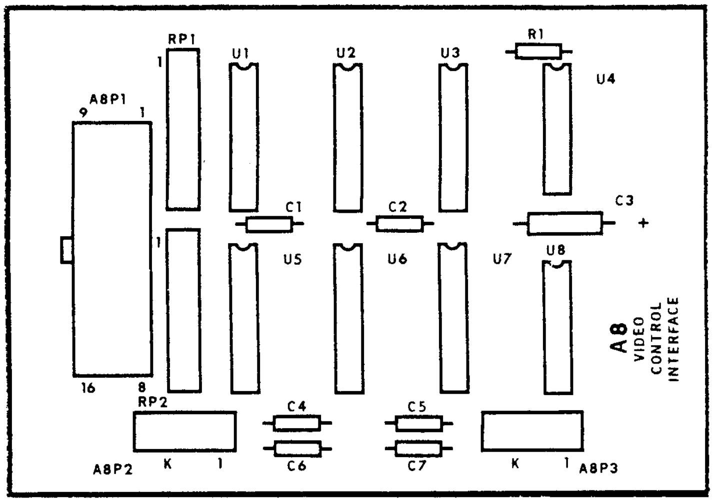


VIDEO BOARD ASSEMBLY (A1), SCHEMATIC DIAGRAM, SHEET 8 OF 8

X. WIRING AND SCHEMATIC DIAGRAMS, PARTS LISTS

VIDEO CONTROL INTERFACE ASSEMBLY (A8)

COMPONENT LOCATION

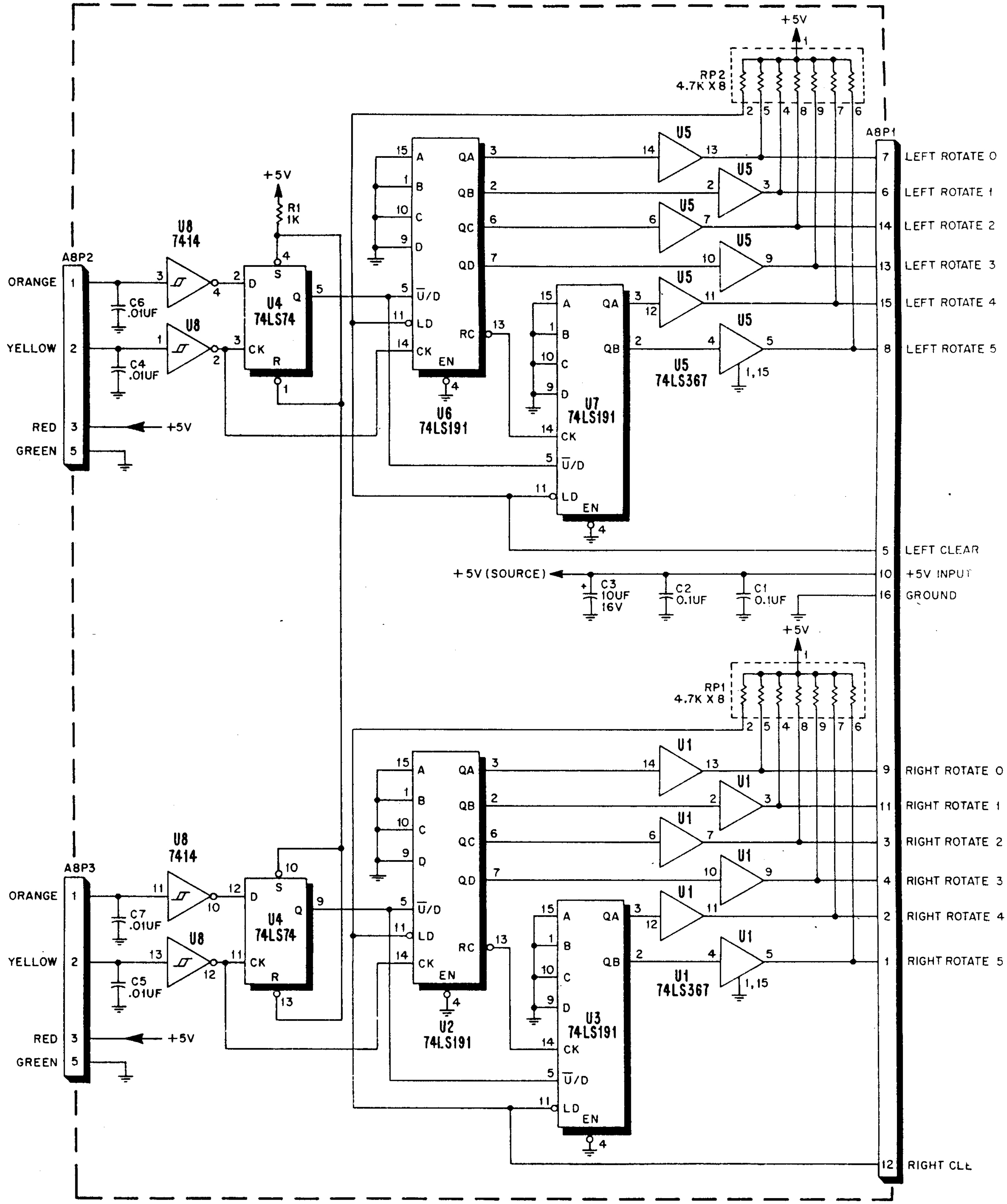


VIDEO CONTROL INTERFACE ASSEMBLY (A8)

PARTS LIST

REFERENCE	DESCRIPTION	PART NUMBER
	VIDEO CONTROL INTERFACE ASSEMBLY (A8)	MA-1385
C1,C2	CAPACITOR, 0.1UF, +80-20%,50V	XO-230
C3	CAPACITOR, 10UF,16V	XO-846
C4-C7	CAPACITOR, .01UF, +80-20%,50V	XO-229
R1	RESISTOR, 1K OHM, 5%, 1/4W	XO-5
RP1,RP2	RESISTOR PACK, 4.7K OHM X 8	XO-161
U1,U5	IC, 74LS367, HEX BUFFER	XO-444
U2,U3,U6,U7	IC,UP/DOWN COUNTER, 74LS191	XO-116
U4	IC, DUAL D FLIP-FLOP, 74LS74	XO-434
U8	IC, HEX INVERTER SCHMITT TRIGGER	XO-397
A8P1	HEADER, 16 PIN	XO-915
A8P2,A8P3	HEADER, 5 PIN	XO-1002
	SUPPORT,(4)	23984

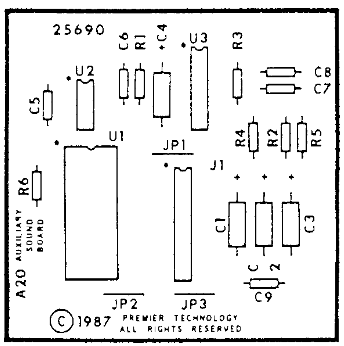
X. WIRING AND SCHEMATIC DIAGRAMS, PARTS LISTS



VIDEO CONTROL
INTERFACE ASSEMBLY (A8)
SCHEMATIC DIAGRAM

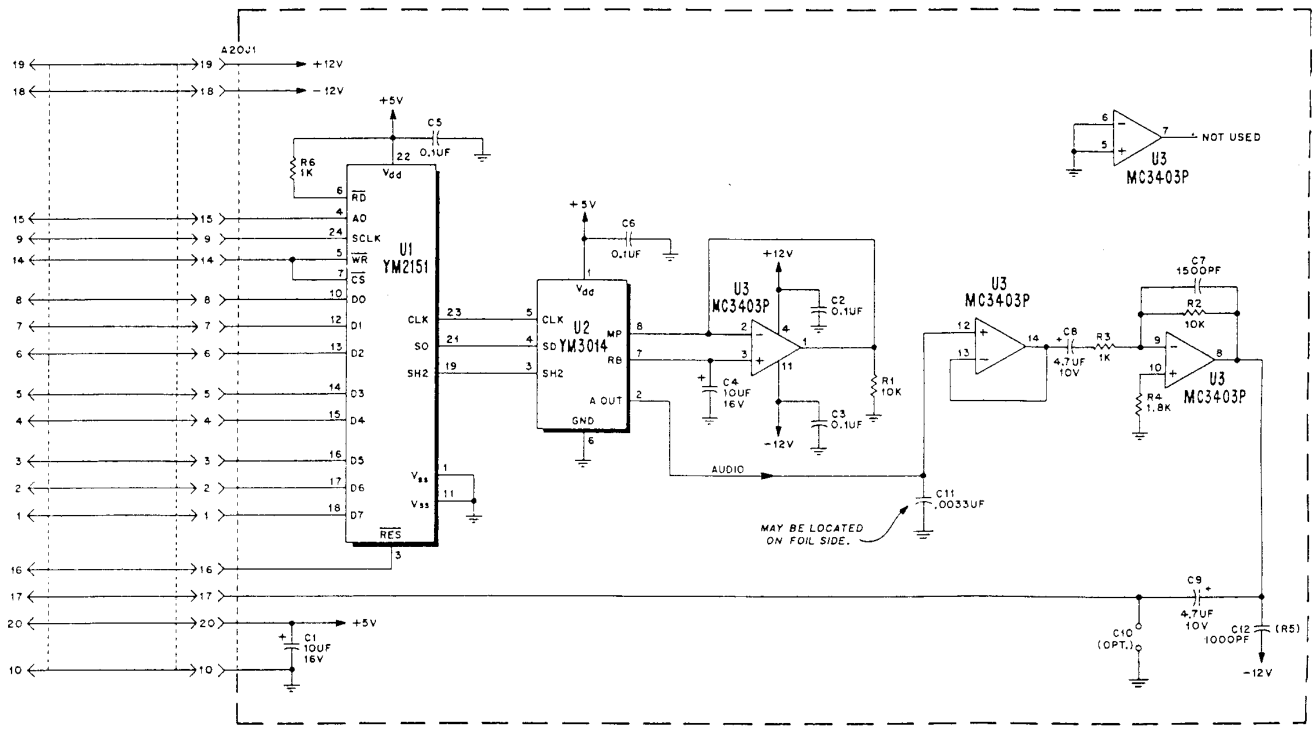
X. WIRING AND SCHEMATIC DIAGRAMS, PARTS LISTS

AUXILIARY SOUND BOARD (A20) COMPONENT LOCATION



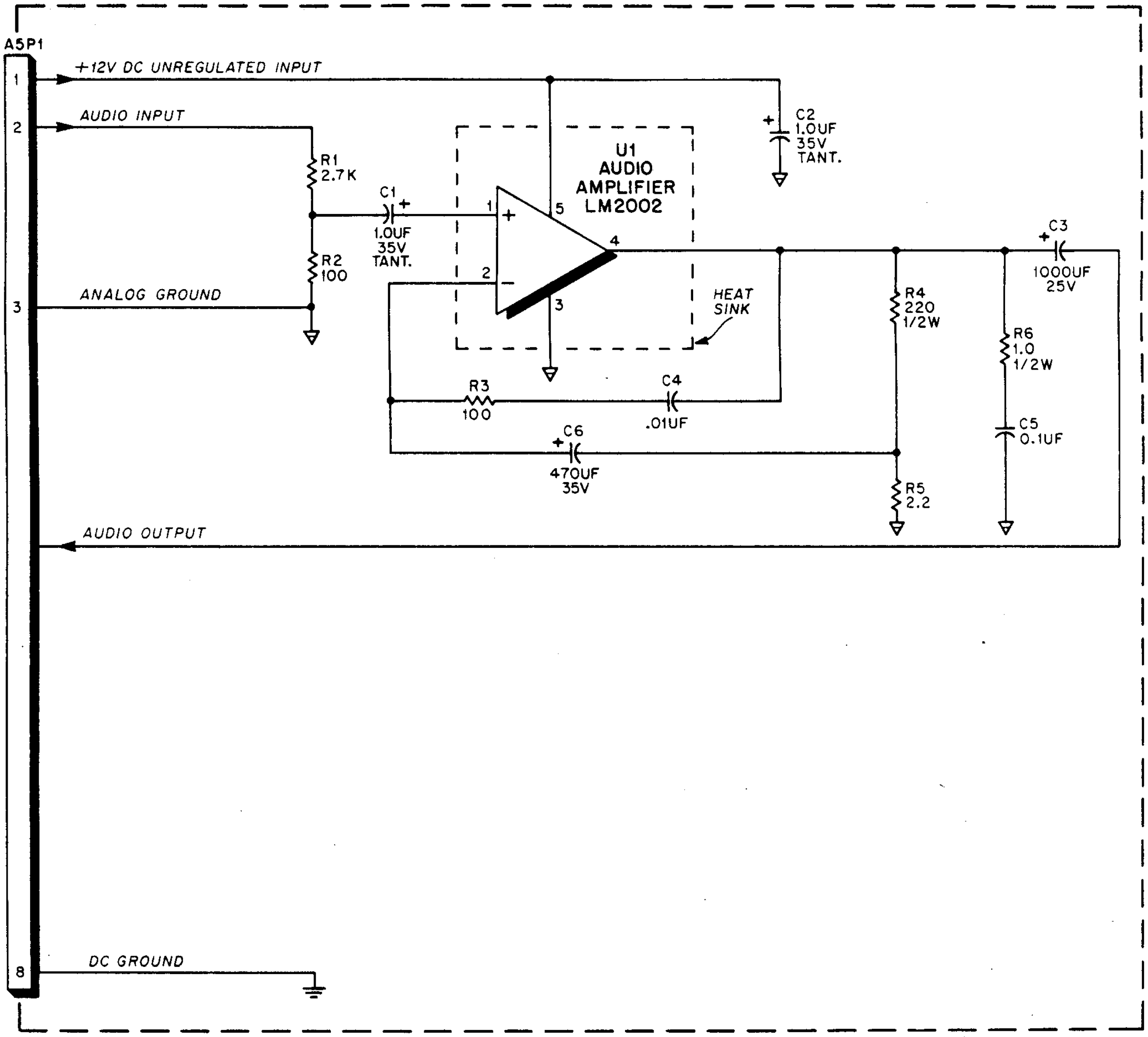
AUXILIARY SOUND BOARD (A20) PARTS LIST

REFERENCE	DESCRIPTION	PART NUMBER
	AUXILIARY SOUND BOARD	MA-1294
C1,C4	CAPACITOR, 10UF, +80%-20%, 16V	XO-846
C2,C3,C5,C6	CAPACITOR, 0.1UF, +80%-20%, 50V	XO-230
C7	CAPACITOR, 1500PF, 5%, 50V	XO-954
C8,C9	CAPACITOR, 4.7UF, 10%, 10V	XO-226
C11	CAPACITOR, 3300PF, 10%, 100V	XO-600
C12(R5)	CAPACITOR, 1000PF, 10%, 100V	XO-296
R1	RESISTOR, 10K OHM, 5%, 1/4W	XO-18
R2	RESISTOR, 10K OHM, 1%, 1/4W	XO-956
R3,R6	RESISTOR, 1K OHM, 5%, 1/4W	XO-5
R4	RESISTOR, 1.8K OHM, 5%, 1/4W	XO-37
U1	IC, SOUND CHIP, YM2151	XO-882
U2	IC, SERIAL DAC, YM3014	XO-883
U3	IC, QUAD OP-AMP, MC3403P	XO-953
	JUMPER, 22 GAUGE (3)	XO-469
	SOCKET, 20 PIN DIP	XO-491
	SOCKET, 24 PIN DIP	XO-529
	RIBBON CABLE	25699



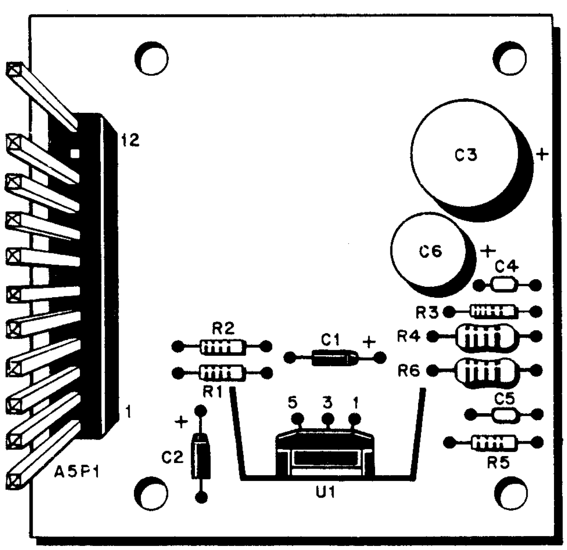
AUXILIARY SOUND BOARD (A20) SCHEMATIC DIAGRAM

X. WIRING AND SCHEMATIC DIAGRAMS, PARTS LISTS



AUXILIARY POWER SUPPLY (A5) SCHEMATIC DIAGRAM

AUXILIARY POWER SUPPLY (A5) COMPONENT LOCATION

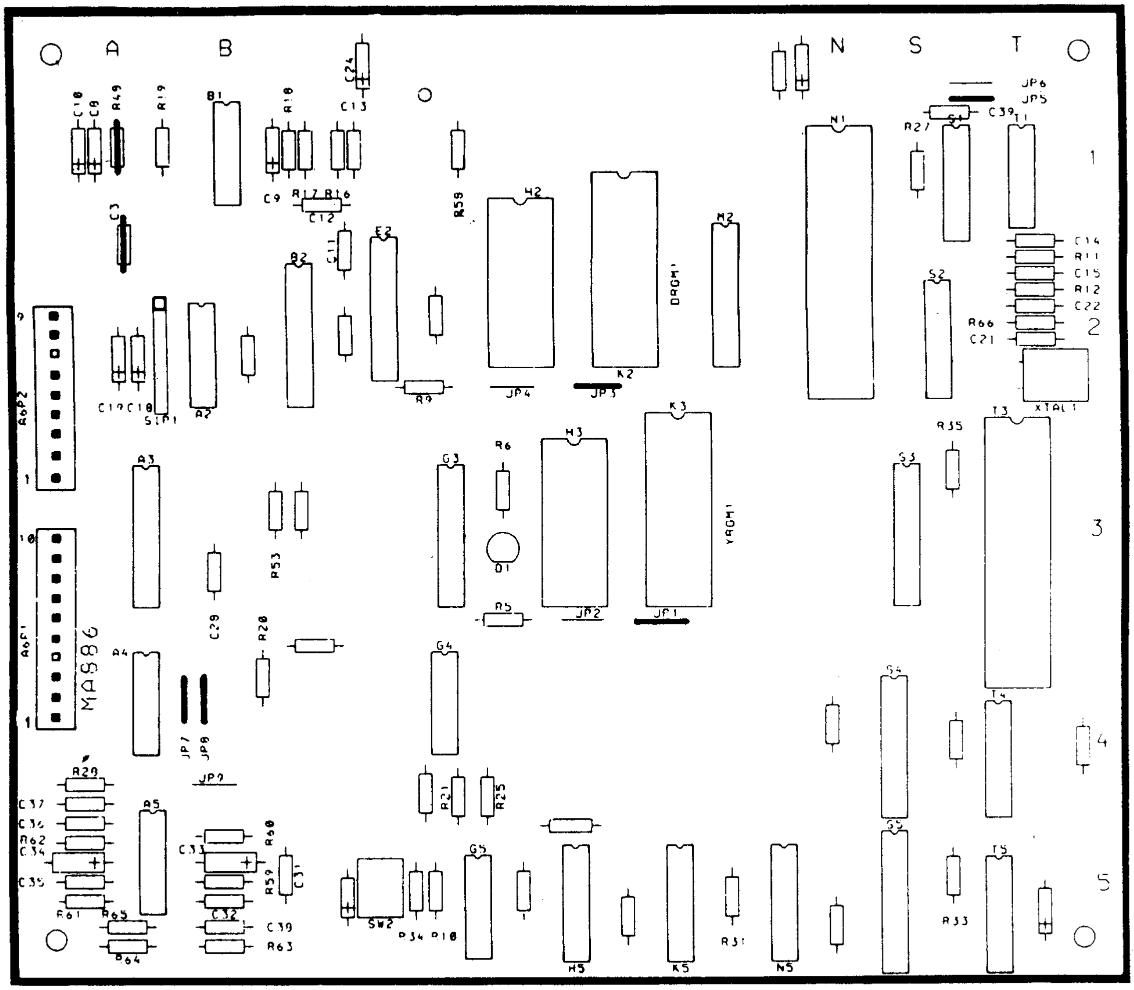


AUXILIARY POWER SUPPLY (A5) PARTS LIST

REFERENCE	DESCRIPTION	PART NUMBER
	AUXILIARY POWER SUPPLY(A5)	MA-1395
C1,C2	CAPACITOR, 1UF, 10%, 35V, TANT.	XO-715
C3	CAPACITOR,1000UF, 25V	XO-874
C4	CAPACITOR, .01UF, +80% -20%, 50V	XO-229
C5	CAPACITOR, 0.1UF, +80% -20%, 50V	XO-230
C6	CAPACITOR, 470UF, 35V	XO-284
R1	RESISTOR, 2.7K Ohm, 5% 1/4W	XO-6
R2,R3	RESISTOR, 100 Ohm, 5%, 1/4W	XO-28
R4	RESISTOR, 220 Ohm, 5%, 1/2W	XO-185
R5	RESISTOR, 2.2 Ohm, 5%, 1/4W	XO-595
R6	RESISITOR, 1 Ohm, 5%, 1/2W	XO-593
U1	AUDIO AMPLIFIER, LM2002	XO-550
	HEAT SINK	XO-472
	12 POSITION CONNECTOR	XO-879

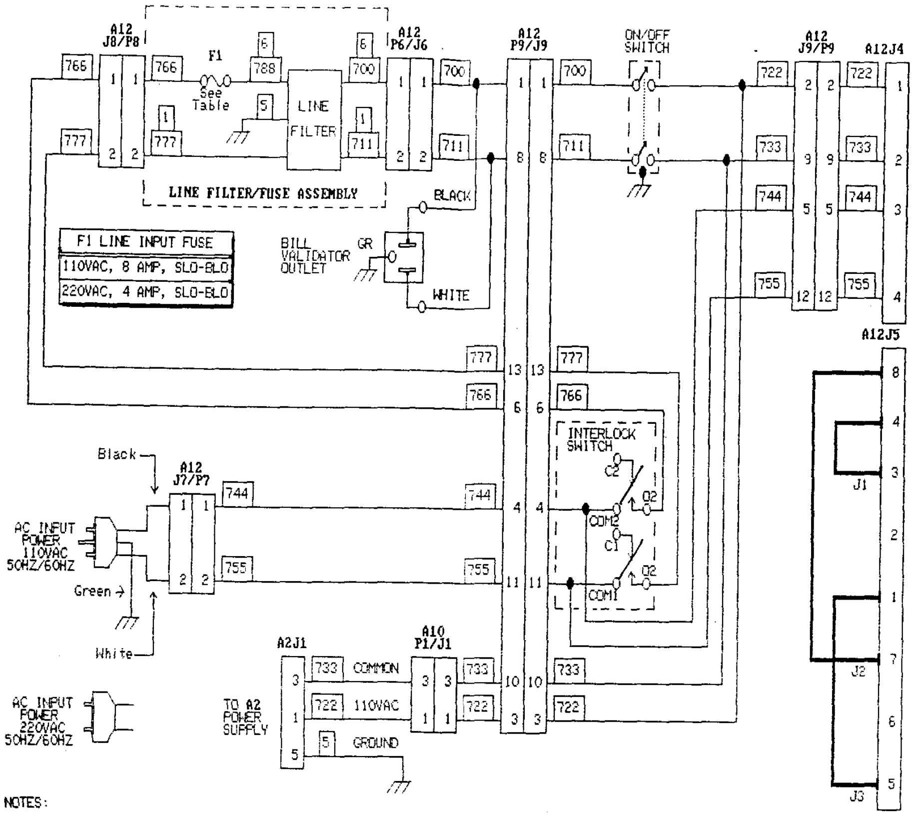
X. WIRING AND SCHEMATIC DIAGRAMS, PARTS LISTS

SOUND BOARD (A6) COMPONENT LOCATION



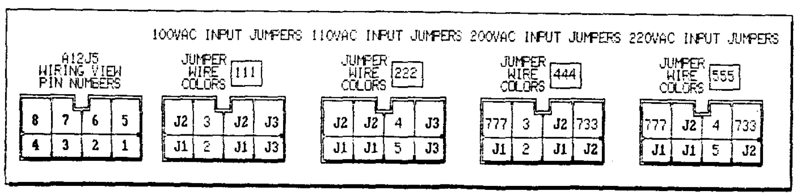
SOUND BOARD (A6) PARTS LIST

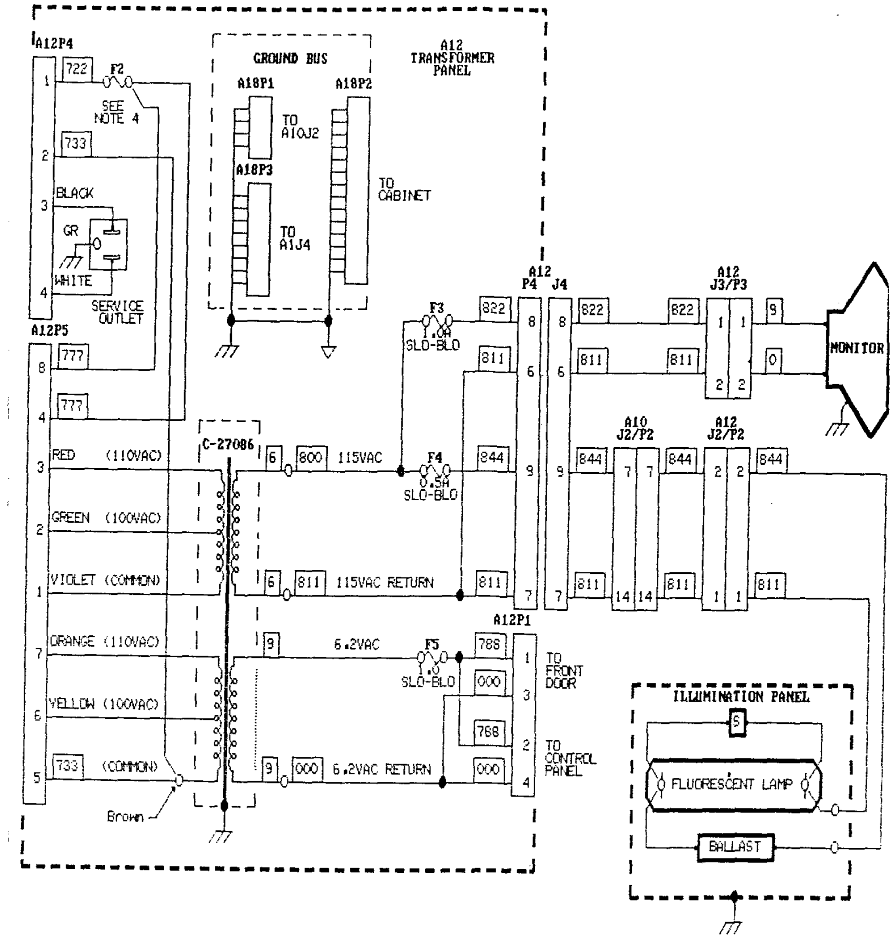
REFERENCE	DESCRIPTION	PART NUMBER
	SOUND BOARD ASSEMBLY (A6)	MA-886-V101
C13,C37	CAPACITOR, 1UF, 20%,50V (NON. POLAR.)	XO-746
C8,C9,C10 C18,C19,C24 C33,C34 AND THREE UNMARKED CAPACITORS	CAPACITOR, 10UF, 20% 25V (TANTALUM)	XO-127
C11,C12	CAPACITOR, 10PF, +80%-20%, 50V	XO-635
C14,C22	CAPACITOR, 33PF, 10%, 100V	XO-896
C15	CAPACITOR, .047UF, 20%, 50V	XO-638
C21	CAPACITOR, 22PF, 10%, 50V	XO-633
C28 AND FOURTEEN UNMARKED CAPACITORS	CAPACITOR, 0.1UF, +80%-20%, 50V	XO-230
C31,C32	CAPACITOR, 0.1UF, 10%, 50V	XO-784
C35	CAPACITOR, 1000PF, 10%, 100V	XO-296
C36	CAPACITOR, 2200PF, 10%, 100V	XO-289
C38	CAPACITOR, 0033UF, 10%, 100V	XO-600
C39	CAPACITOR, 220PF, 10%, 100V	XO-694
D1	DIODE, MV5752, (LED,RED)	XO-270
R5,R9,R10, R27,R28,R31, R33,R35	RESISTOR, 1K Ohm, 5%, 1/4W	XO-5
R5	RESISTOR, 240 Ohm, 5%, 1/4W	XO-173
R11,R12	RESISTOR, 470 Ohm, 5%, 1/4W	XO-35
R21,R25	RESISTOR, 3K Ohm, 5%, 1/4W	XO-23
R16,R17,R58	RESISTOR, 10K Ohm, 5%, 1/4W	XO-18
R18	RESISTOR, 6.8K Ohm, 5%, 1/4W	XO-8
R20,R34	RESISTOR, 4.7K Ohm, 5%, 1/4W	XO-7
R61,R62, R63,R64	RESISTOR, 33K Ohm, 5%, 1/4W	XO-43
R59,R60	RESISTOR, 100K Ohm, 5%M 1/4W	XO-45
R65	RESISTOR, 27K Ohm, 5%, 1/4W	XO-11
A2	IC, 7430, 8 INPUT NAND GATE	XO-643
A3,B2,S5	IC, 74LS374, OCTAL "D" FLIP FLOP	XO-96
A4	IC, 74LS74, DUAL "D" FLIP FLOP	XO-434
A5,B1	IC, MC3403P, QUAD OP-AMP	XO-953
E2	IC, AD7528J, MULTIPLIER DAC	XO-647
G3	IC, 74LS377, OCTAL "D" FLIP FLOP	XO-97
G4,T1	IC, 74LS04, HEX INVERTER	XO-418
G5	IC, 74HC08, QUAD 2 INPUT "AND" GATE	XO-872
H2,H3	IC, 6116LP-15, 2K X 8 RAM	XO-928
H5,K5,N5, S1,T5	IC, 74LS161, SYNCHRONOUS PRESETTABLE BINARY COUNTER	XO-440
K2,K3	IC, SPECIFIED PER GAME	
M2	IC, 74LS245, OCTAL BUS TRANSCEIVER	XO-79
N1,T3	IC, 6502A, CPU	XO-893
S2	IC, 74LS139, DUAL 1 OF 4 DECODER	XO-419
S3	IC, 74HCT245, OCTAL BUS TRANSCEIVER	XO-891
T4	IC, 74LS138, 1 OF 8 DECODER	XO-437
SIP 1	RESISTOR PACK 8 X 1K OHM	XO-493
SW2	SWITCH, PUSHBUTTON	XO-897
XTAL1	CRYSTAL, 4 MHZ	XO-366
A6P1,A6P2	CONNECTOR	XO-879
	28 PIN DIP SOCKET (2)	XO-536
	JUMPER, 22 GUAGE (6)	XO-469
	20 PIN DIP SOCKET	XO-491



NOTES:

1. A12J5 SHOWN IN 110VAC OPERATION
2. CHANGE A12J5 JUMPERS FOR 220VAC OPERATION
3. CHANGE INTERNALLY A2 POWER SUPPLY FOR 220VAC OPERATION
4. PRIMARY POWER FUSE VALUES
   110VAC 5.0 AMP SLO-BLO
   220VAC 2.5 AMP SLO-BLO
5. [xxx] INDICATES WIRE COLOR
6. CIRCUIT GROUND
7. EARTH GROUND

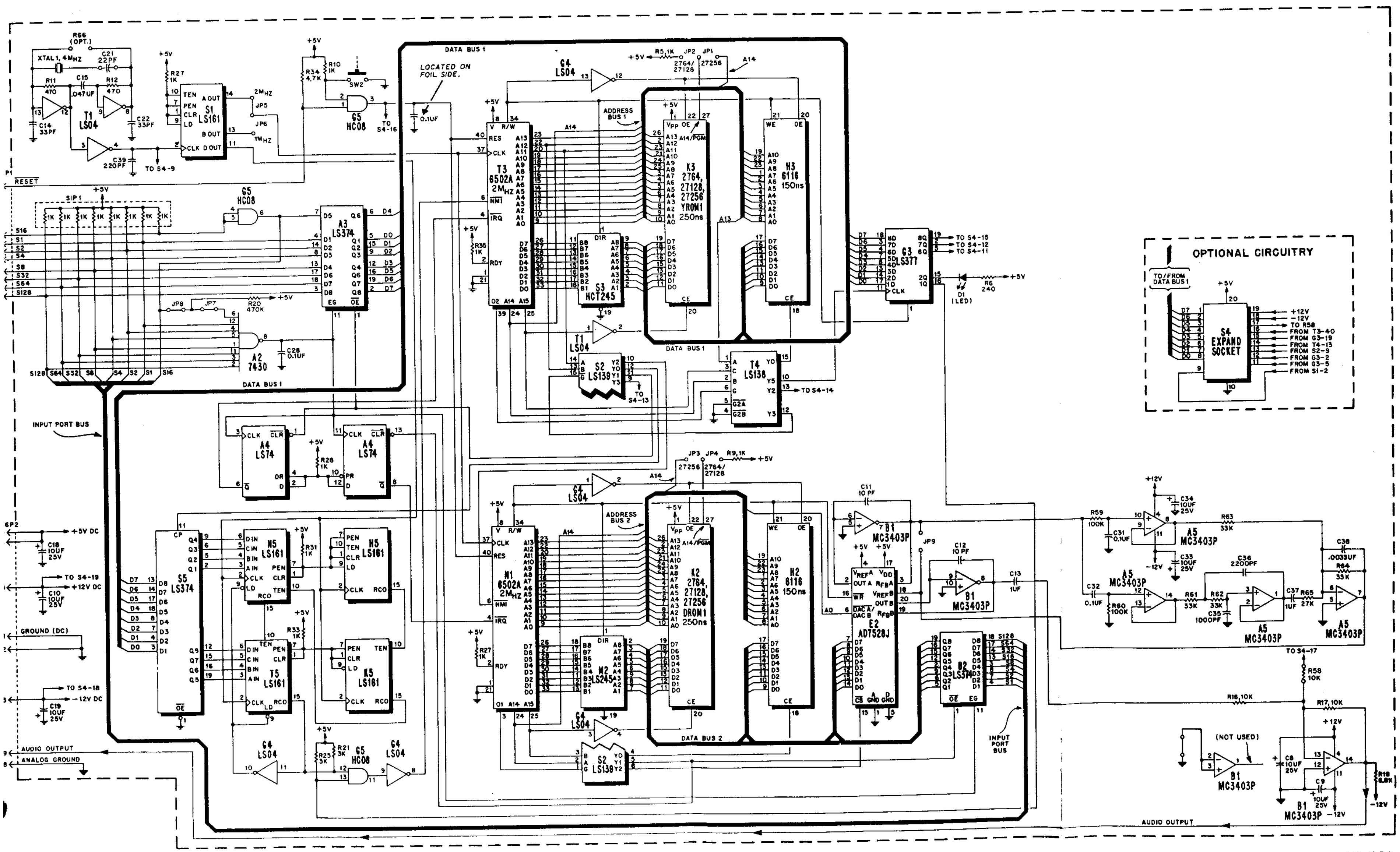




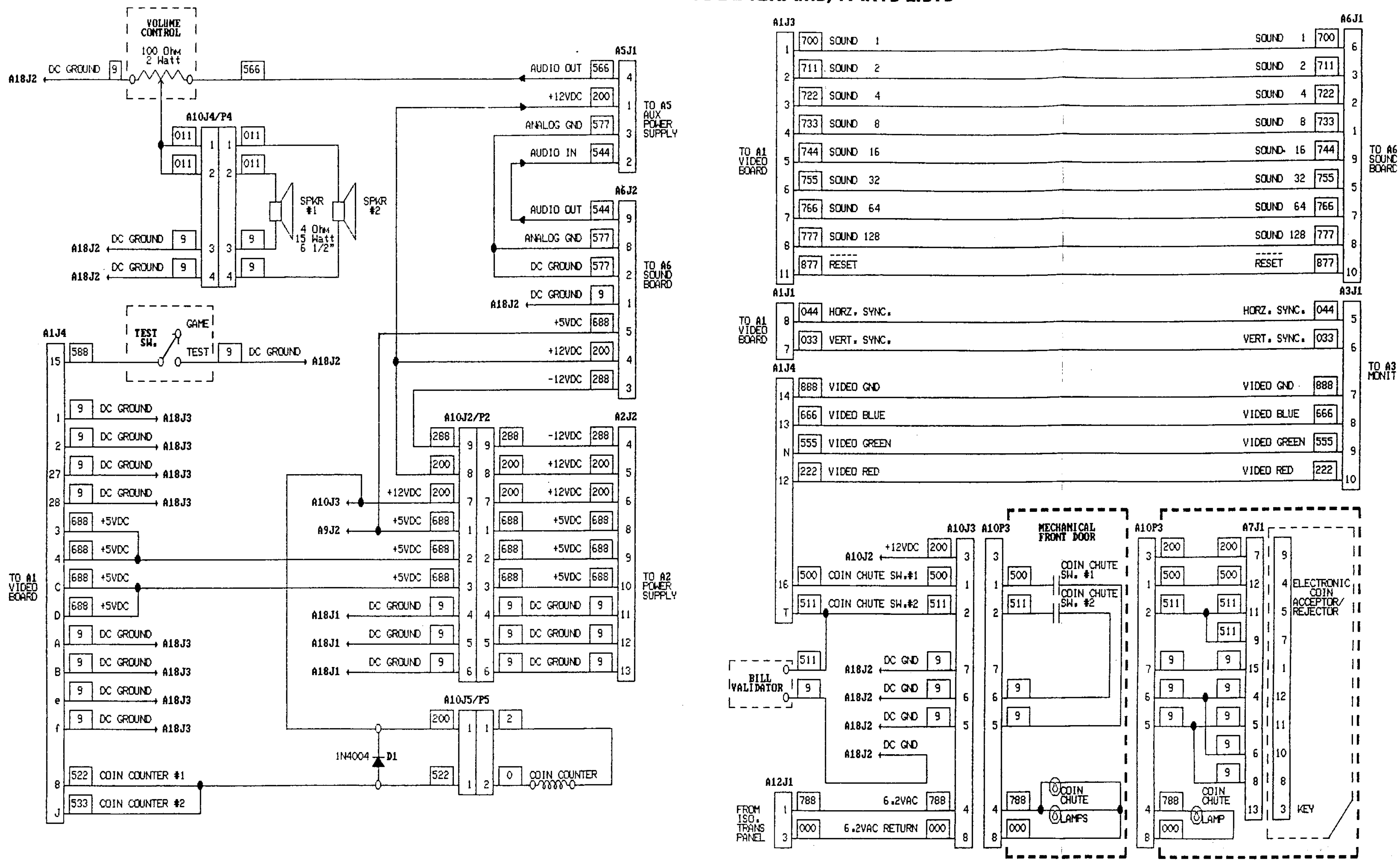
FUSE DESIGNATIONS	
F1	LINE INPUT (See Table)
F2	PRIMARY POWER (See Note 4)
F3	MONITOR (115VAC)
F4	FLUORESCENT LAMP (115VAC)
F5	ILLUMINATION (6.2VAC)

COLOR CODE			
0	BLACK	5	GREEN
1	BROWN	6	BLUE
2	RED	7	VIOLET
3	ORANGE	8	GRAY
4	YELLOW	9	WHITE

TRANSFORMER PANEL SCHEMATIC/WIRING DIAGRAM

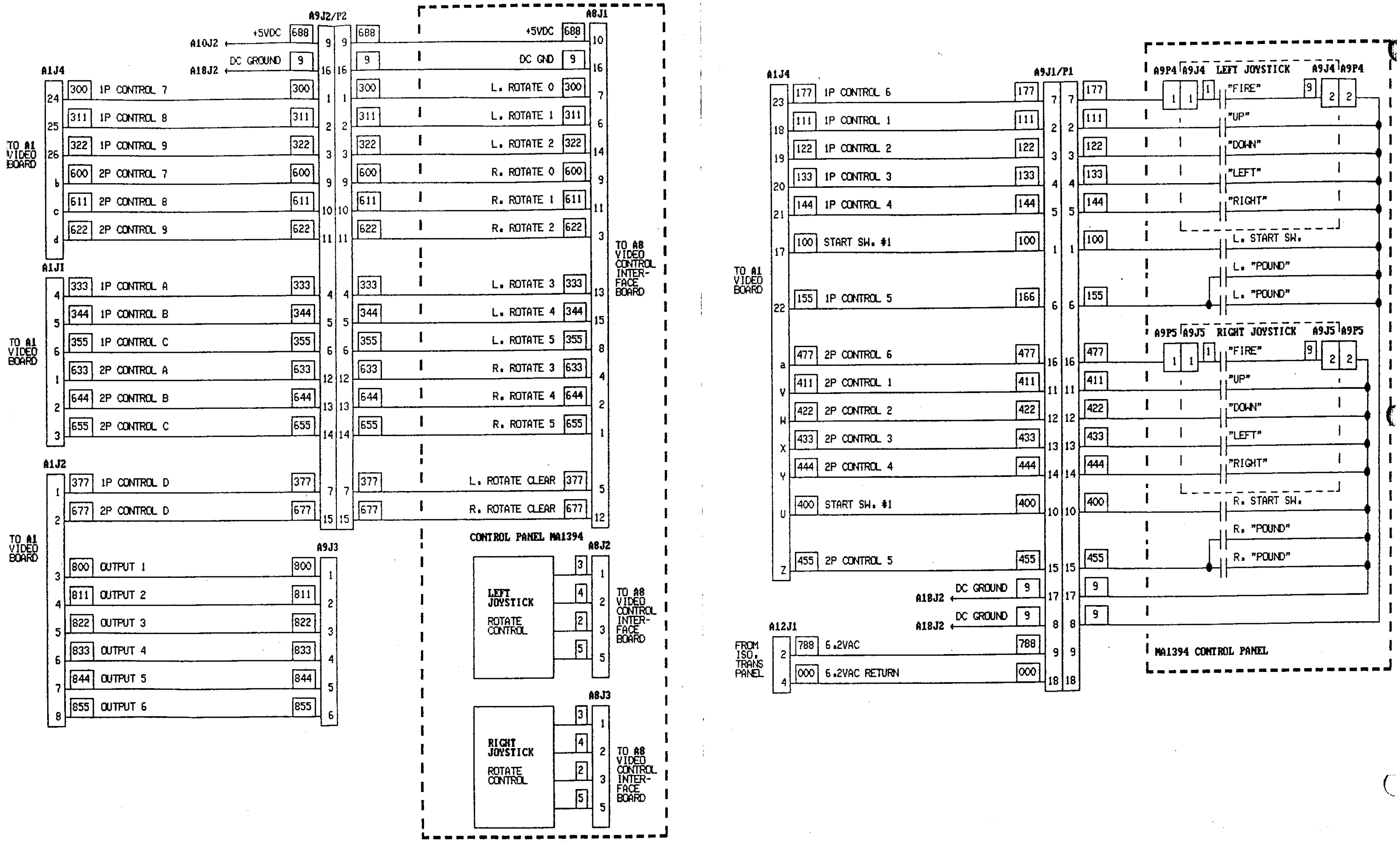


SOUND BOARD (A6) SCHEMATIC DIAGRAM



CABINET SCHEMATIC/WIRING DIAGRAM, SHEET 2 OF 2

X. WIRING AND SCHEMATIC DIAGRAMS, PARTS LISTS



CABINET SCHEMATIC/WIRING DIAGRAM, SHEET 1 OF 2